

SCOTT



SERVICE MANUAL

Model: LCT32SHA

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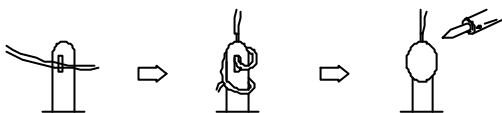
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This manual is the latest at the time of printing, and does not
include the modification which may be made after the printing,
by the constant improvement of product.
.....

I. Safety Instructions

 <div style="border: 1px solid black; padding: 5px; text-align: center;">CAUTION RISK OF ELECTRIC SHOCK DO NOT OPEN</div> 	<p>The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.</p> <p>The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.</p>
<p>CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.</p>	

PRECAUTIONS DURING SERVICING

- In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements. Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
- Use specified internal Wiring. Note especially:
 - Wires covered with PVC tubing
 - Double insulated wires
 - High voltage leads
- Use specified insulating materials for hazardous live parts. Note especially:
 - Insulating Tape
 - PVC tubing
 - Spacers (insulating barriers)
 - Insulating sheets for transistors
 - Plastic screws for fixing micro switches
- When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



- Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
- Check if replaced wires do not contact sharply edged or pointed parts.
- Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can. Please leave them at an appropriate depot.



SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this TV receiver. The following are the necessary instructions to be observed before servicing.

- An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
- Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
- To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.

4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.
5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high temperature components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.

Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15 μ F AC type capacitor, between a good earth ground (water pipe, conductor etc..) and the exposed metallic parts, one at a time.


Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.

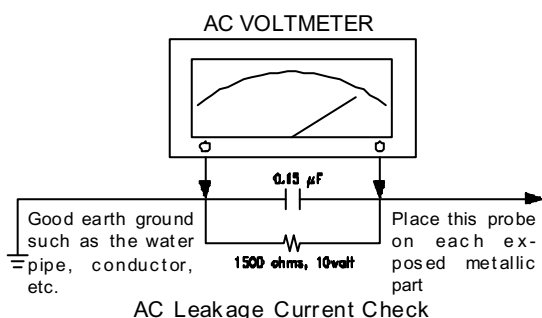
The measured voltage must not exceed 0.3V RMS.

This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.

The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this TV receiver have special safety-related characteristics. These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc. The replacement parts which have these special safety characteristics are identified by  marks on the schematic diagram and on the parts list. Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, X-RAY RADIATION or other hazards.



1. Do not power on.

1.1 Please check AC cable if connect to AC plug.

Is true the connector don't connect to AC plug. Please connect it.

2.2 Please check AC cable if connect to AC power.

Is true the AC cable don't connect to AC power. Please connect it.

3.3 Please check power board of fuse if broken.

If the F1 fuse is broken, Please pull out the AC cable from AC power. Please check AC L power and AC N ground by multimeter, The read number is infinite, the fuse is broke. then look up power board if not burn out place. Is true it. Please change power board or be changed power board.

2. The power on switch of green extinguish.

2.1 The power of led(indicator light) is red light, To touch power on key when indicator light wink.

Is true that the power DC output have somewhere short circuit.

Please check connector J39,J31 .If not connector direction is wrong.

Or the mainboard somewhere of power short circuit.

3.The power is normal work ,but don't backlight.

3.1 The indicator light work normal (green light).

Please check Main board of transistor Q1&collect if not has +5v voltage.

Is true Q18 collect hasn't +5v ,To check Q18 if fail. Or to check Q18 of base if not low.

(Low is working, high don't work).

Please refer to attached sheet A circuit diagram.

3.2 Please check backlight of connector if not it direction is wrong or the connector of wire compositor direction is wrong.

3.3 To check connector panel of voltage is +24v. It's true .Then to check of the first pin if it have +5V voltage, It's true , than to check power board of +24v voltage ,It's true. The panel of backlight board is fail. The change panel of backlight board.

Please refer to attached sheet B Panel of datasheet.

4.The screen don't have picture But have backlight.

4.1 To check to panel of voltage ,To check main board of bead L69 and L57 connect if not OK.Then check the L69 and L57 of voltage is +12v(27 inch panel voltage is +5v, To check L68 and L56) . Next to check fuse F1 and connector J10 if not is +12v(27 inch panel voltage is +5v). If isn't please check power board of connector CON5 if has +12v(27 inch panel voltage is +5v).

4.2To check to main board +12 V voltage. To check to main board IC U35 of the first pin if

+5v voltage ,It's fail. It's low (close 0 v) working.

The circuit diagram follow down:

Please refer to attached sheet A circuit diagram.

5.The remote control don't be control.

6.1 The check batteries of remote control if it run out of .

6.2 To check main board of connector J21 of wire connect fastness and the connector of wire open.

Please refer to attached sheet A circuit diagram.

6.The sound don't output.

7.1 To check main board +24v voltage of connector J8 ,It's true not +24v voltage. Then to check power main +24v fail .

Please refer to attached sheet A circuit diagram.

7.The DTV don't detect .

7.1 To check mainboard of connector J24 and DTV mainboard of connector HA1 of FCC wire if no connect fastness.

Please refer to attached sheet C of DTV circuit diagram.

Product Specification

Product Model:	LCT37SHA
Screen Size:	37" diagonal
Screen Area:	819.6mm(H) x 460.8mm(V)
Aspect Ratio:	16:9
External Size:	925.8mm(W) x 708.0mm(H) x 240.0mm(D) (with Stand)
Gross Weight:	24 kg
Resolution:	1366 (H) x 768 (V) pixels (Each pixel has R/G/B 3 color cells)
Pixel Dot Pitch:	0.6mm(H) x 0.6mm(V)
Color:	16.7 millions of colors (R/G/B each 256 scales)
Gray Scale:	256 (R/G/B each 8-bit)
Peak Brightness:	500cd/m ²
Contrast (Dark Room):	1000:1 (Typical)
TV System:	NTSC M, ATSC
Sound:	Mono, Stereo, SAP (BTSC)
Sound Effect:	Acoustic Cinema Enhancement
Power Supply:	AC 120V, 60Hz
Power Consumption:	230W
Input/Output Terminal:	Antenna Input (F Type) x 2 (NTSC & ATSC)
	RS-232 (D-Sub 9 Pin Type) x 1 (Only for DTV)
	VGA (D-Sub 15 Pin Type) x 1
	HDMI (Ver 1.1) connector x 1
	Component Video - YPbPr x 2 (RCA Terminals)
	Video Input (RCA Terminals) x 1
	S-Video Input Mini Din 4 Pin Terminal x 1
	Stereo, Audio x 5
	1 set of Audio Output terminals (RCA, L&R)
	SPDIF (Optical) x 1 (Only for ATSC)
Agent System:	UL, cUL, FCC

NOTE:

- *The specifications shown above may be changed without notice for quality improvement.*

Support the Signal Mode

A. D-Sub Mode (VGA)

Resolution	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
640 x 480	31.50	60.00
	37.86	72.81
800 x 600	35.16	56.25
	37.90	60.32
	48.08	72.19
1024 x 768	48.40	60.00

B. HDTV Mode (YPbPr)

Resolution	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
480i	15.734	59.94
480p(720x480)	31.468	59.94
720p(1280x720)	45.00	60.00
1080i(1920x1080)	33.75	60.00

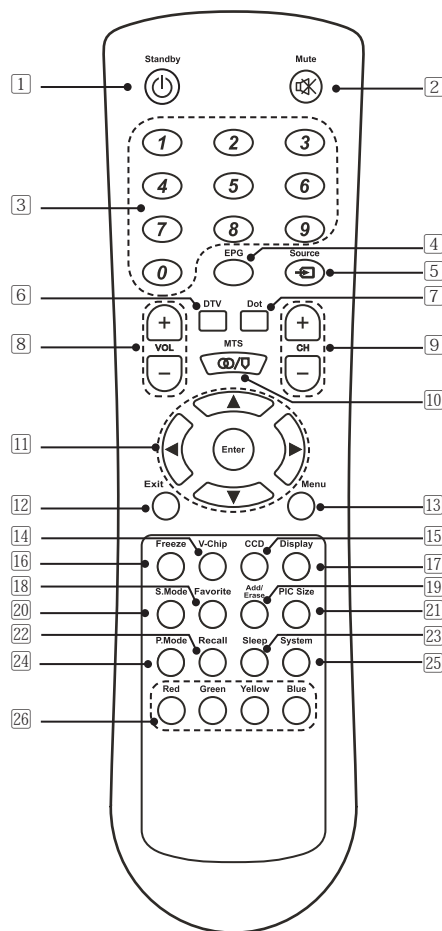
C. HDMI Mode

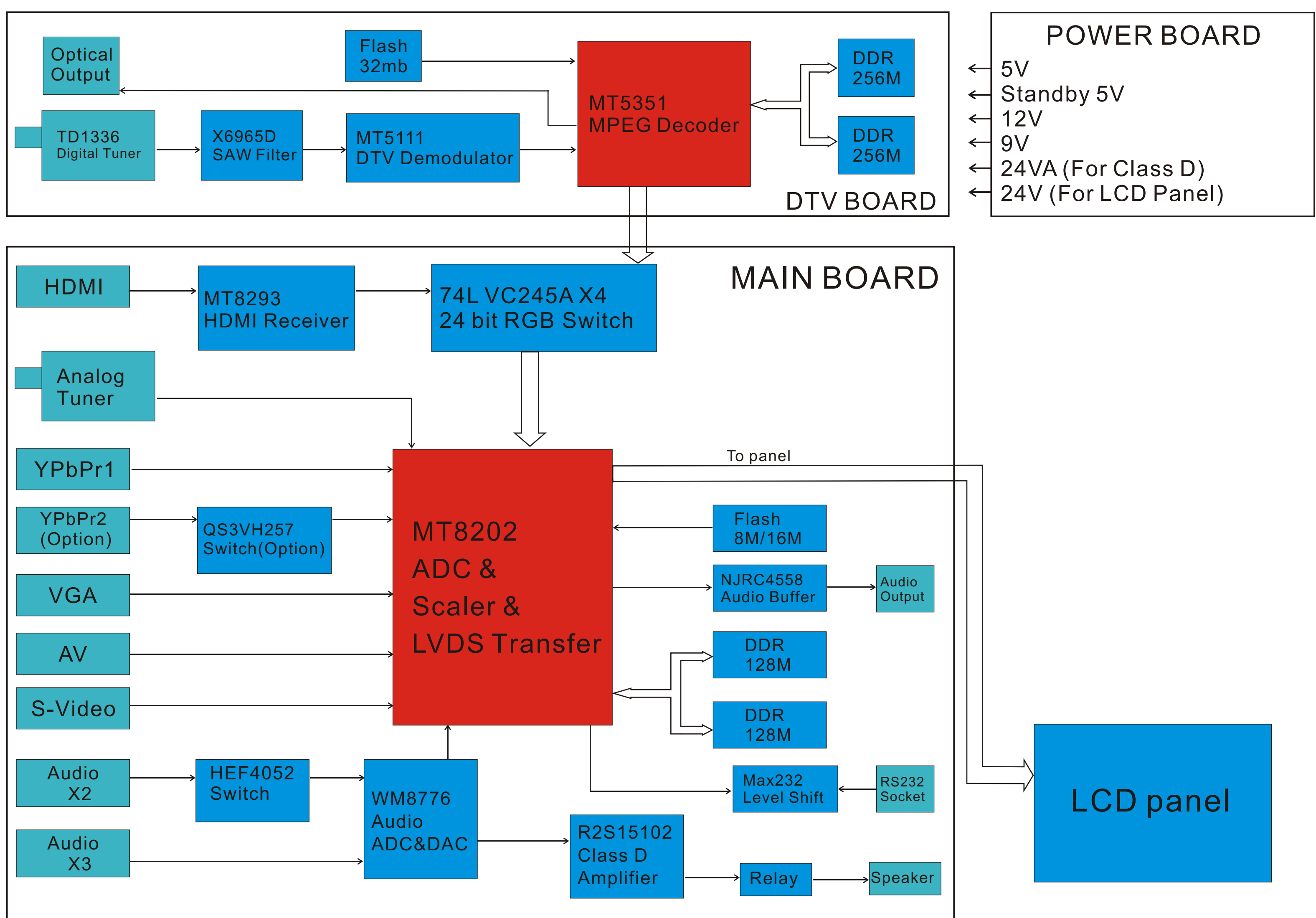
Resolution	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
480p	31.468	59.94
720p	45.00	60.00
1080i	33.75	60.00

- When the signal received by the Display exceeds the allowed range, a warning message shall appear on the screen.
- You can confirm the input signal format from the on-screen.

Remote Control

- 1 **Power** (⏻): Press to turn on and off.
- 2 **Mute** (🔇): Press to mute the sound.
Press again or press **VOL +/-** to restore the sound.
- 3 **0~9 Number Buttons**: In TV mode, press 0~9 to select a channel; the channel changes after 2 seconds.
- 4 **EPG**: Press to display EPG (Electronic Program Guide) menu.
- 5 **Source** (📶): Press to select the signal sources.
- 6 **DTV**: Press to select Digital TV mode.
- 7 **Dot**: Press number buttons with it to select the channels directly in DTV.
- 8 **VOL +/-**: Press to adjust the volume.
- 9 **CH +/-**: Press to change channels.
- 10 **MTS**: Press to repeatedly cycle through the Multi-channel TV sound (MTS) options. Such as Stereo, Mono, or Separate Audio Program (SAP broadcast).
- 11 **◀, ▲, ▼, ▶, Enter**: Press **◀, ▲, ▼, ▶** to move the on-screen cursor. To select an item, press **Enter** to confirm.
- 12 **Exit**: Press to return or exit the OSD menu.
- 13 **Menu**: Press to display the OSD menu.
- 14 **V-Chip**: Press to select the child protect mode.
- 15 **CCD**: Press to select the Closed Caption mode.
- 16 **Freeze**: Press to freeze the picture, press again to restore the picture.
(This button is not available for VGA mode.)
- 17 **Display**: Press to display the channel information and it disappears after 3 seconds.
- 18 **Favorite**: Press repeatedly to cycle through the favorite channel list.
- 19 **Add/Erase**: Press to add or delete favorite channel.
- 20 **S.Mode**: Adjust the TV sound by selecting one of the preset factory settings, such as Normal, News, Cinema, Concert, or User.
- 21 **PIC.Size**: Press to change the screen size, such as Full, 4:3, Panoramic. (Note: In VGA mode, it can select picture size is Full. While in DTV mode, it can select picture size is: Full and 4:3.)
- 22 **Recall**: Press to return to previous channel.
- 23 **Sleep**: Press to sleep a time for the TV to turn off automatically, such as 15Min, 30Min, 60Min, 90Min, 120Min and, OFF. To cancel sleep time, press Sleep repeatedly until sleep OFF appears.
- 24 **P.Mode**: Adjust the TV picture by selecting one of the preset factory settings, such as Hi-Bright, User, Cinema, Normal and Vivid.
- 25 **System**: Press repeatedly to cycle through the system options: AUTO, NTSC3.58 and PAL. (This button is activated for AV, S-Video input source.)
- 26 **Color Buttons**:
Red: Press this button to access the red item or page.
Blue: Press this button to access the blue item or page.
Green: Press this button to access the green item or page.
Yellow: Press this button to access the yellow item or page.



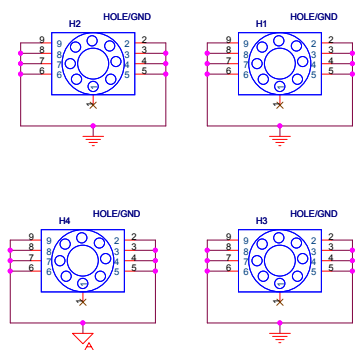
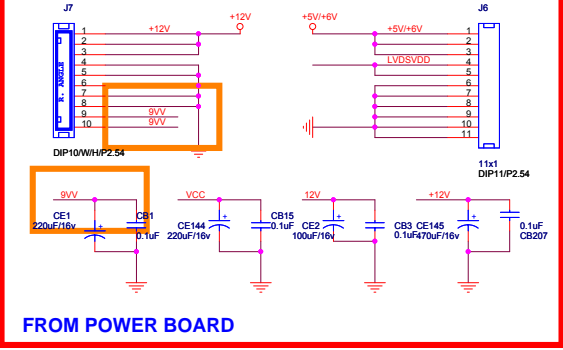
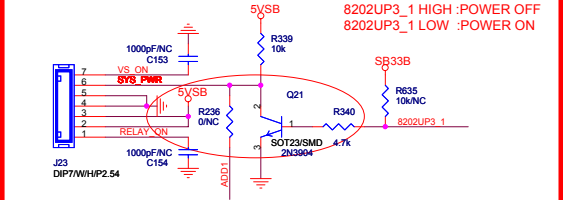
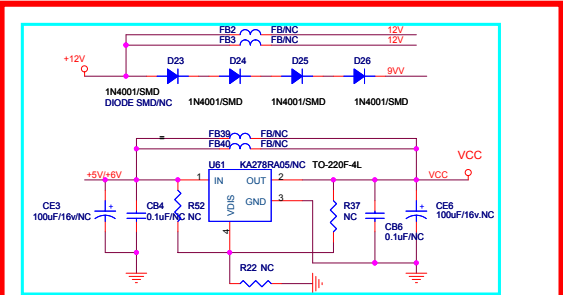
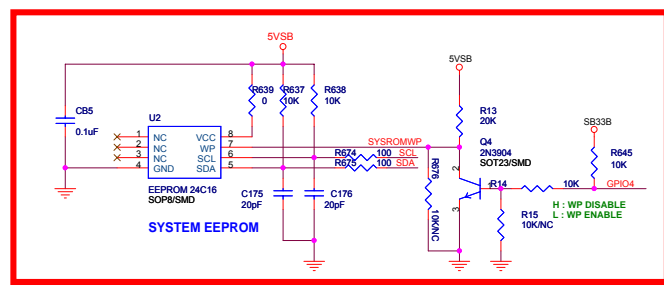
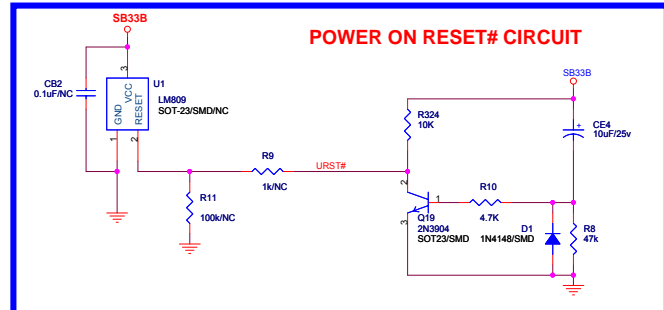
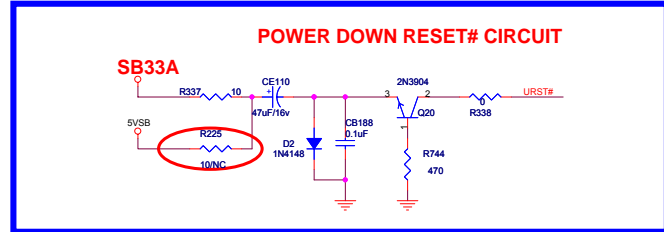
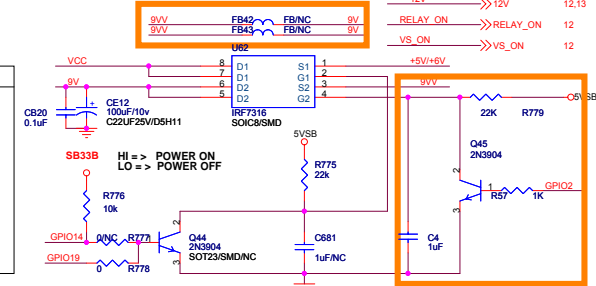


MT8202E (PBGA388) LCDTV BOARD 4 LAYERS FOR AKAI

1. INDEX / POWER / RESET / EEPROM
2. LDO
3. MT8202E PBGA388
4. MT8202 DECOUPLING
5. DDR MEMORY & FLASH
6. MT5351 INTERFACE
7. HDMI MT8293
8. DAUGHTER BOARD IN
9. WM8776 & VIDEO BYPASS
10. AUDIO / VIDEO IN CIRCUIT
11. VGA & PC AUDIO IN
12. LVDS OUT
13. BACK LIGHT / KEYPAD
14. TUNER IN
15. AV IN
16. AUDIO IN
17. AUDIO Amplifier

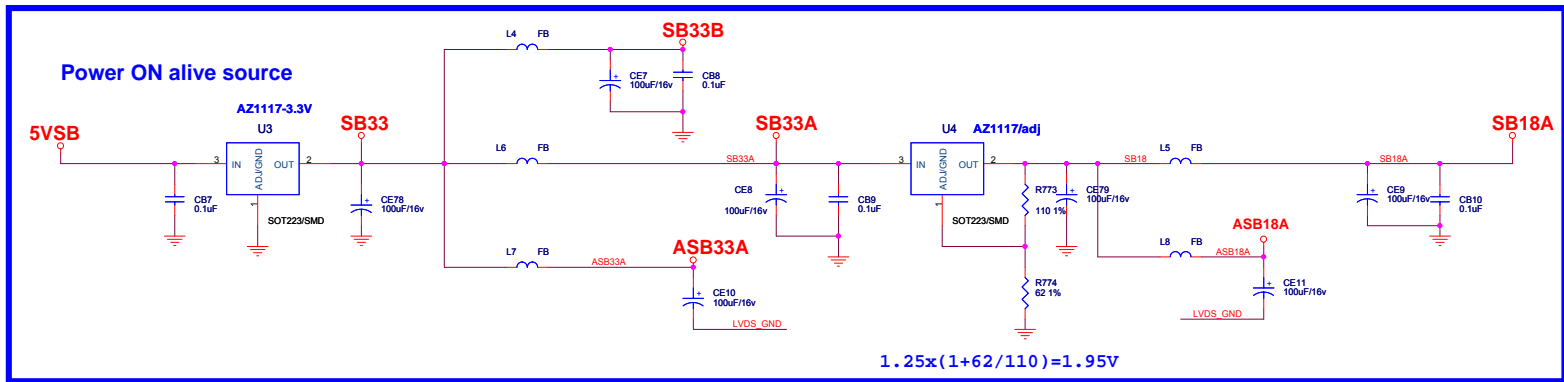
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SCL	>>SCL	9,14
SDA	>>SDA	9,14
URST#	>>URST#	3
8202UP3_1	>>8202UP3_1	3
GPIO2	>>GPIO2	3,12
GPIO4	>>GPIO4	3
GPIO14	>>GPIO14	3,13
GPIO19	>>GPIO19	3,13
9V	>>9V	7,9,14
12V	>>12V	12,13
RELAY_ON	>>RELAY_ON	12
VS_ON	>>VS_ON	12

Rev	History	P#	Date
AKAI_MT8202_27US_LVDS_V0.0	New		2005/11/22
AKAI_MT8202_27US_HDMI_LVDS_V0.0	ADD HDMI / VIDEO /AUDIO CONNECTOR INPUT IN		

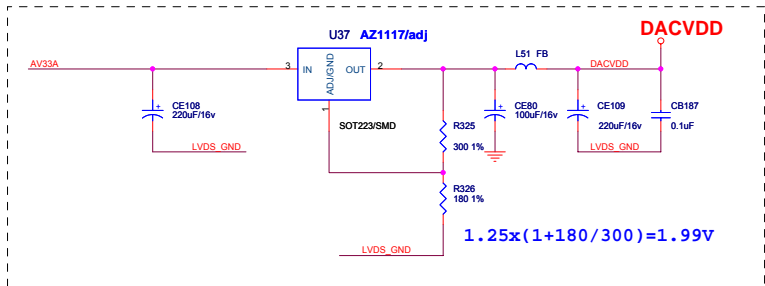
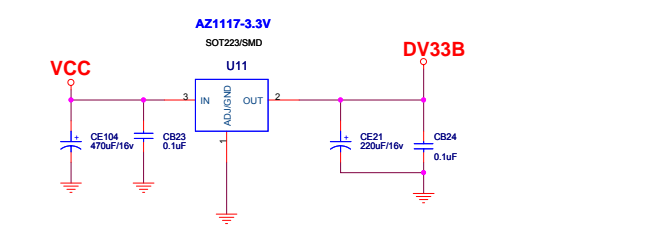
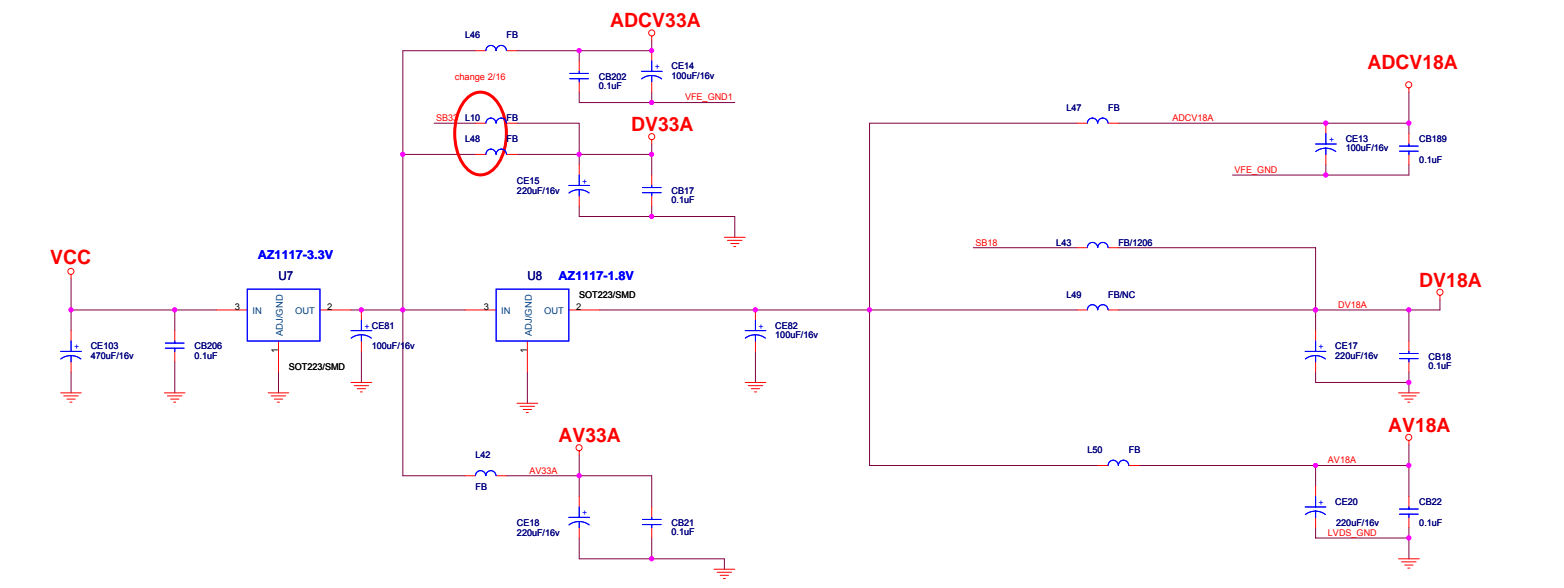


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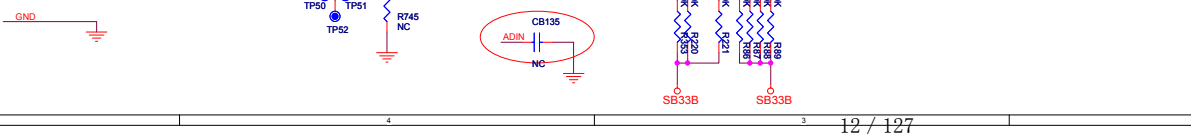
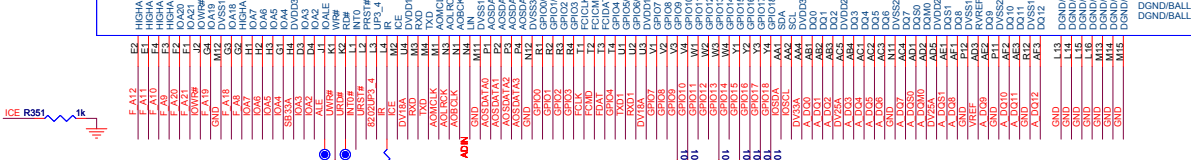
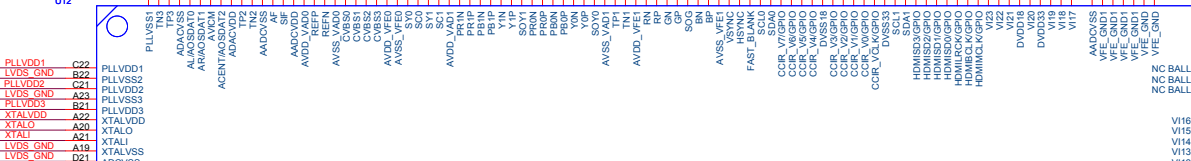
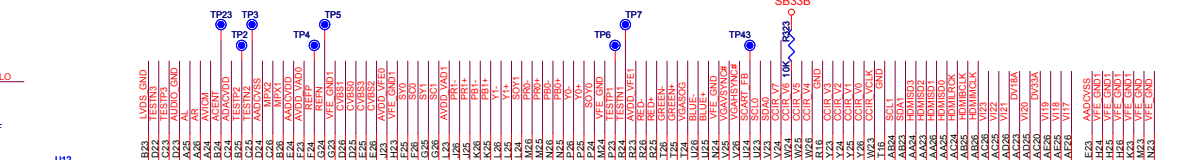
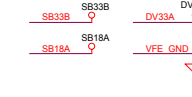
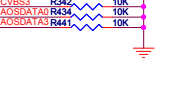
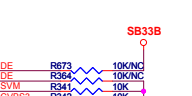
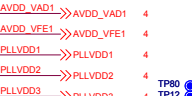
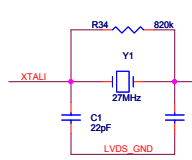


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- VFE_GND >>> VFE_GND 3.4.8.11
- VFE_GND1 >>> VFE_GND1 3.4.8.11

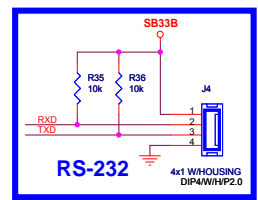


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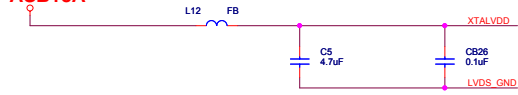
MT8202 SOCKET



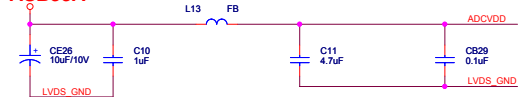
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- ADCVDD >> ADCVDD 3
- AVICM >> AVICM 3
- PWM2VREF >> PWM2VREF 3
- DACFS >> DACFS 3
- LVDDA >> LVDDA 3
- LVddb >> LVddb 3
- LVDDC >> LVDDC 3
- AVDD_VFE0 >> AVDD_VFE0 3
- AVDD_VAD0 >> AVDD_VAD0 3
- AADCVD0 >> AADCVD0 3
- ADACVDD >> ADACVDD 3
- VPLLVD01 >> VPLLVD01 3
- VPLLVD02 >> VPLLVD02 3
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- AVDD_VFE1 >> AVDD_VFE1 3
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- DACVDDC >> DACVDDC 3
- TESTP3 >> TESTP3 3
- TESTN3 >> TESTN3 3
- TESTP4 >> TESTP4 3
- TESTN4 >> TESTN4 3
- REFP >> REFP 3
- REFN >> REFN 3
- AADCVSS >> AADCVSS 3.10
- AUDIO_GND >> AUDIO_GND 3.10
- LVDS_GND >> LVDS_GND 2.3,12
- VFE_GND >> VFE_GND 2.3,8,11
- AADCVSS >> AADCVSS 3.10
- VFE_GND1 >> VFE_GND1 2.3,8,11

STANDBY ANALOG POWER

ASB18A

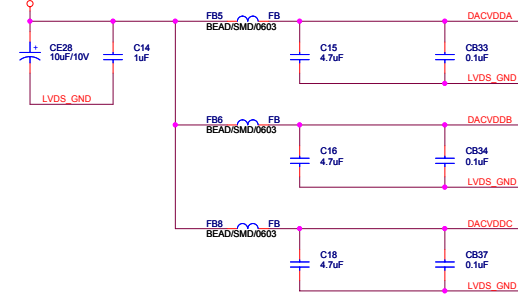


ASB33A



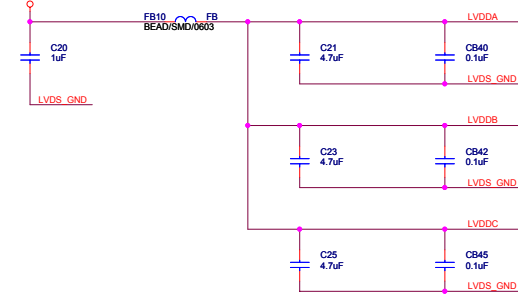
NORMAL VIDEO DAC POWER

DACVDD



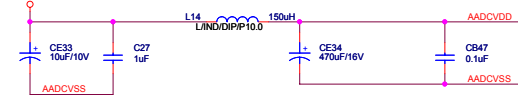
NORMAL VIDEO DAC POWER

AV33A

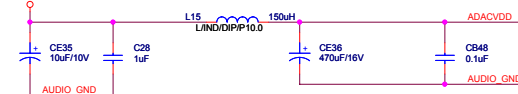


NORMAL AUDIO ADC / DAC POWER

ADC33A

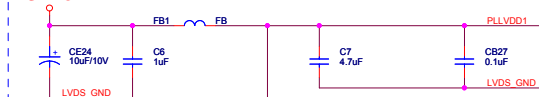


ADC33A

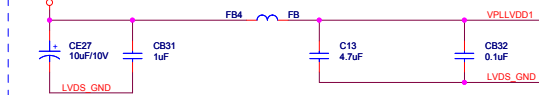


NORMAL ANALOG POWER

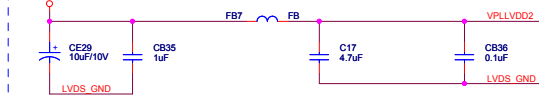
ASB18A



AV18A

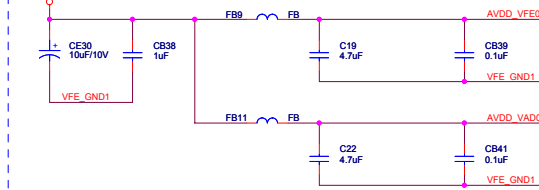


AV33A

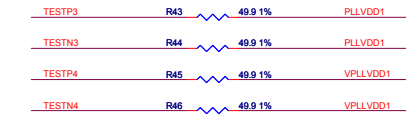
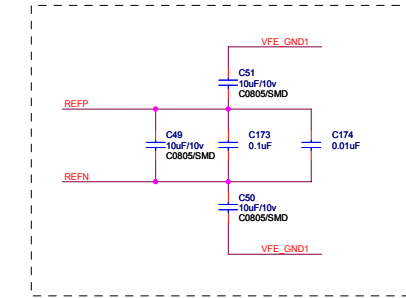
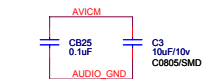
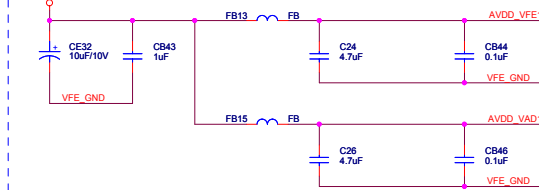


NORMAL VIDEO ADC POWER

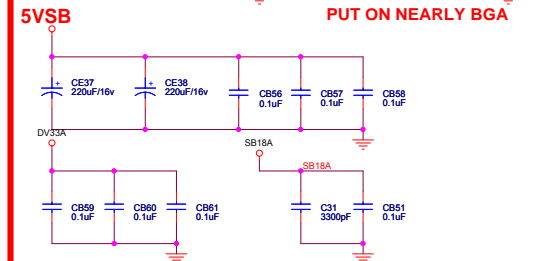
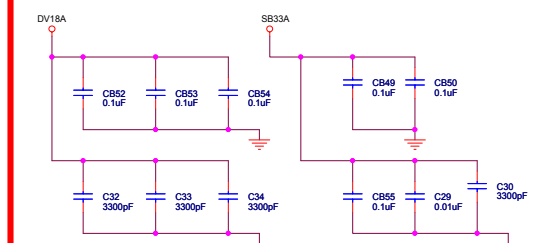
ADC33A



ADC18A

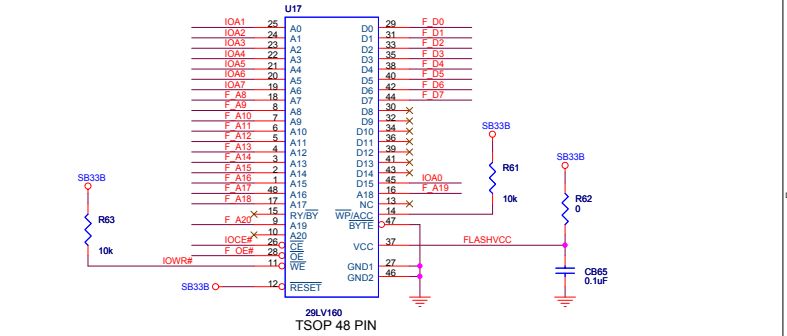
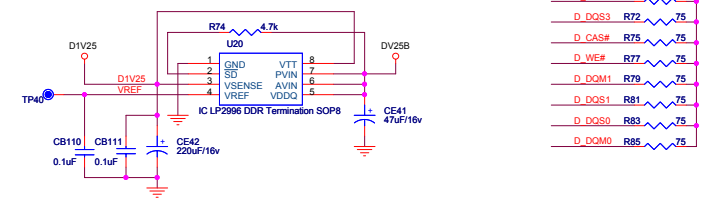
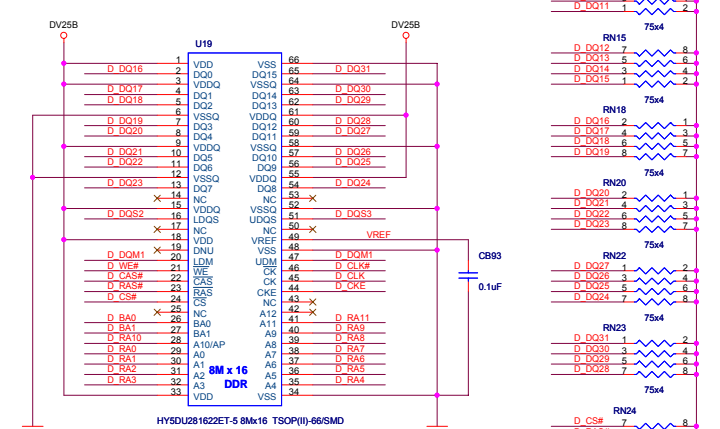
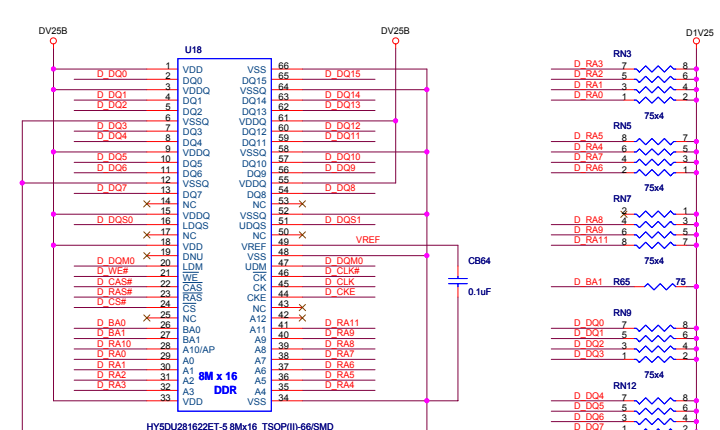
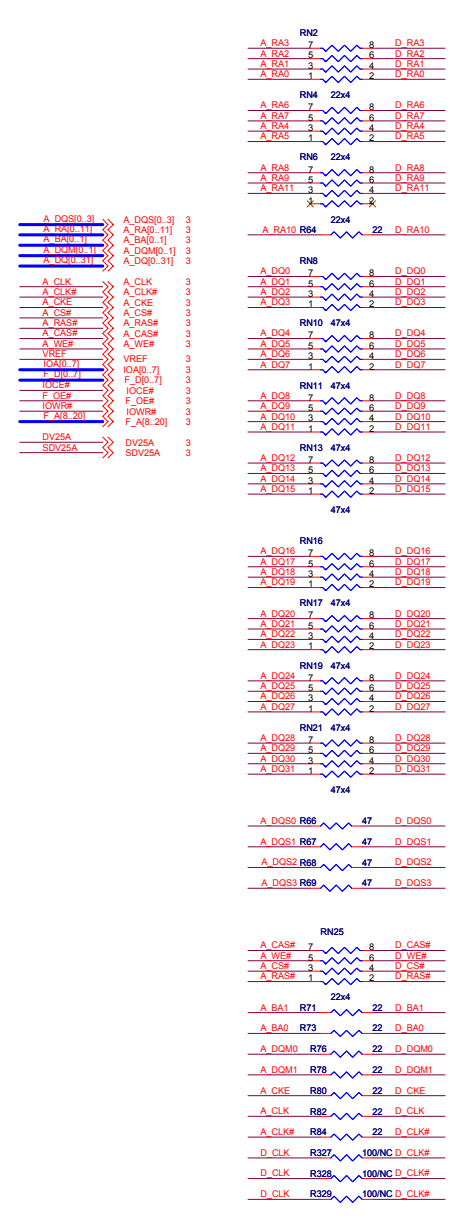


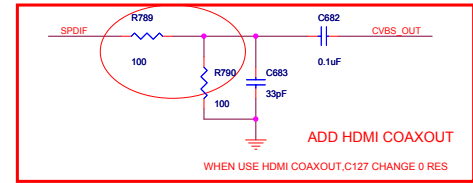
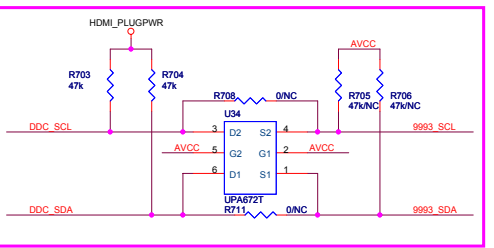
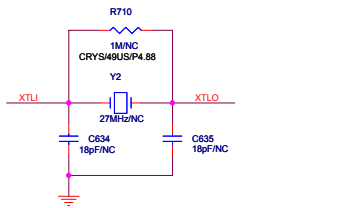
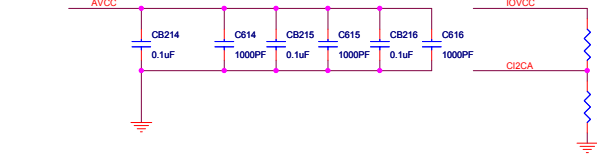
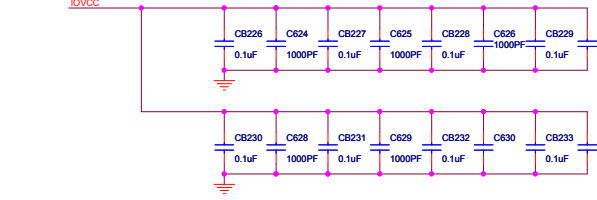
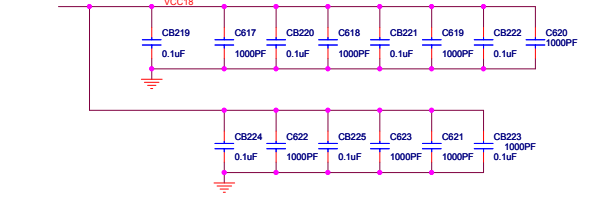
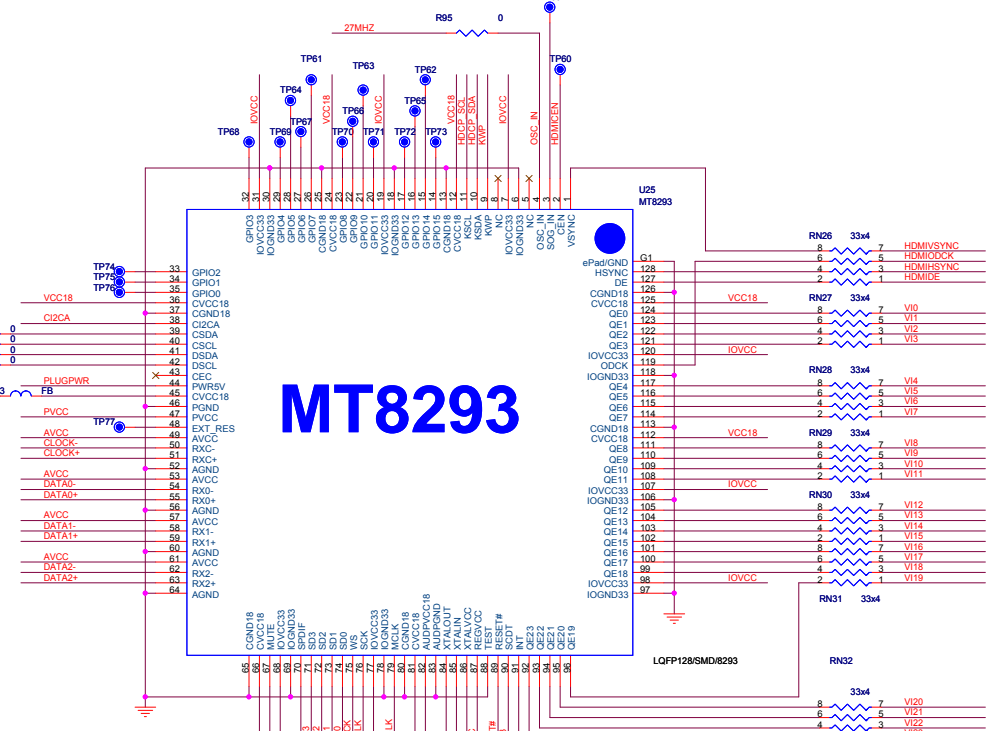
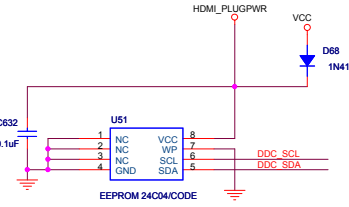
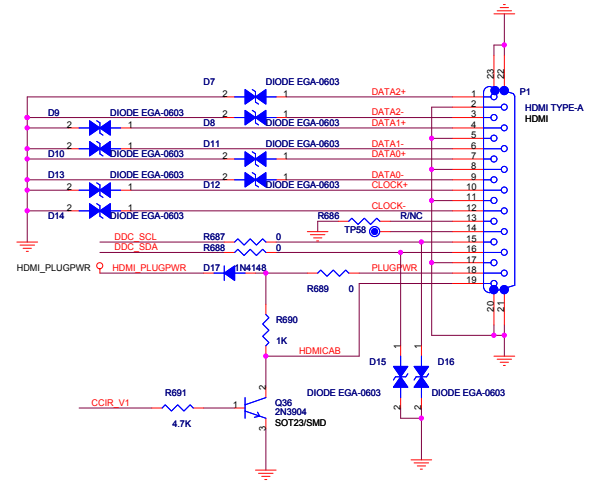
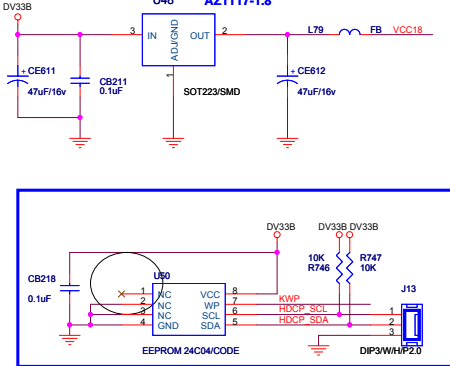
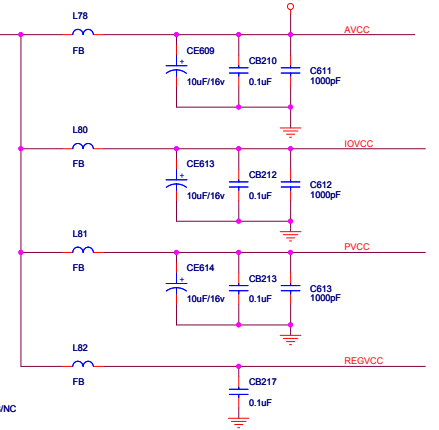
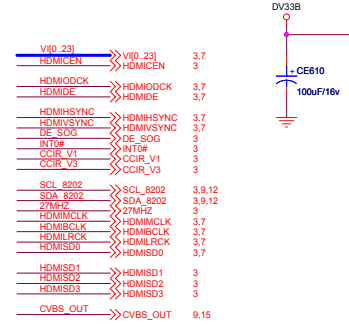
MT8202 DIGITAL POWER & DECOUPLING



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MT8202 DECOUPLING			
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C	AKAI_MT8202_27US_LVDS_V0.0	<Checked>	1
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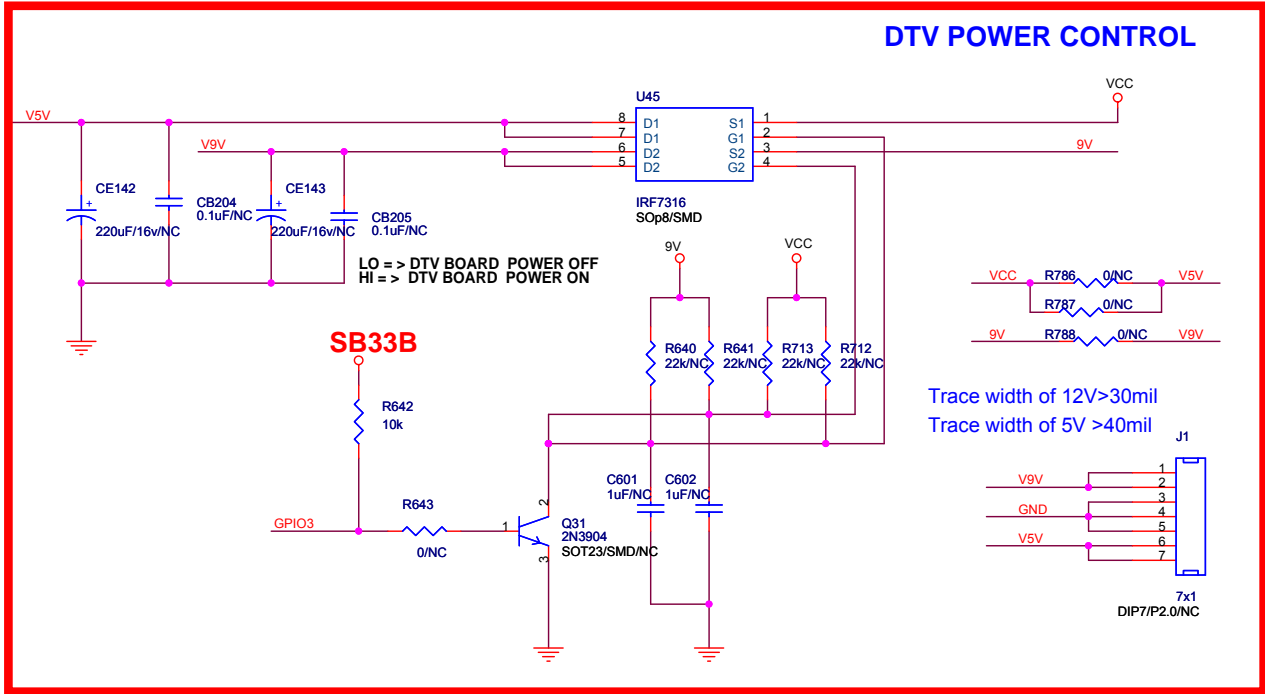
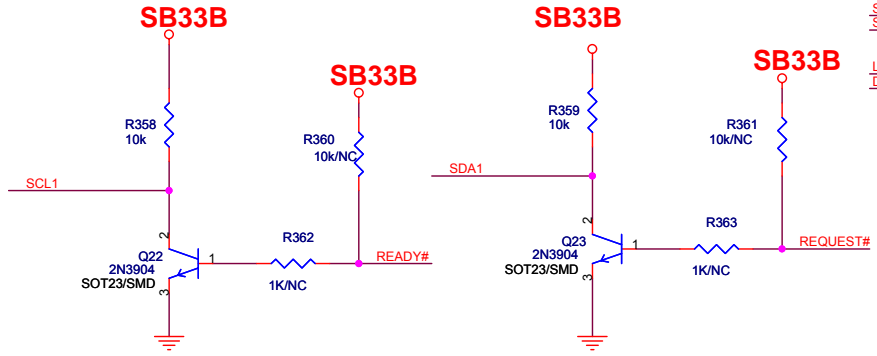




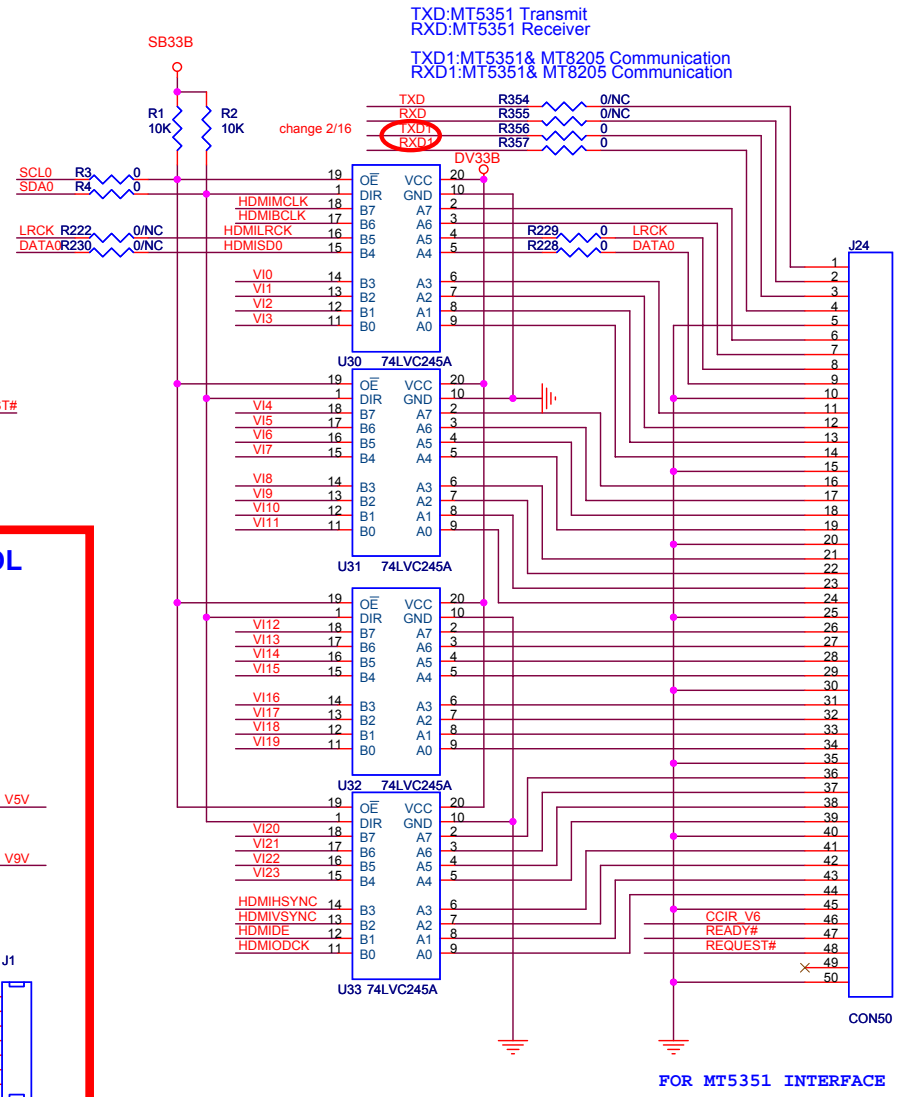
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HDMI INPUT MT8293			
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HDMIMCLK	>>	HDMIMCLK	3,6
HDMIBCLK	>>	HDMIBCLK	3,6
HDMILRCK	>>	HDMILRCK	3,6
HDMISD0	>>	HDMISD0	3,6
HDMIDE	>>	HDMIDE	3,6
HDMIODCK	>>	HDMIODCK	3,6
HDMIHSYNC	>>	HDMIHSYNC	3,6
HDMIVSYNC	>>	HDMIVSYNC	3,6
VI[0..23]	>>	VI[0..23]	3,6
TXD	>>	TXD	3,11
RXD	>>	RXD	3,11
TXD1	>>	TXD1	3
RXD1	>>	RXD1	3
SCL1	>>	SCL1	3
SDA1	>>	SDA1	3
GPIO3	>>	GPIO3	3
CCIR_V6	>>	CCIR_V6	3
SCL0	>>	SCL0	3
SDA0	>>	SDA0	3
9V	>>	9V	1,9,14



Trace width of 12V > 30mil
Trace width of 5V > 40mil



FOR MT5351 INTERFACE

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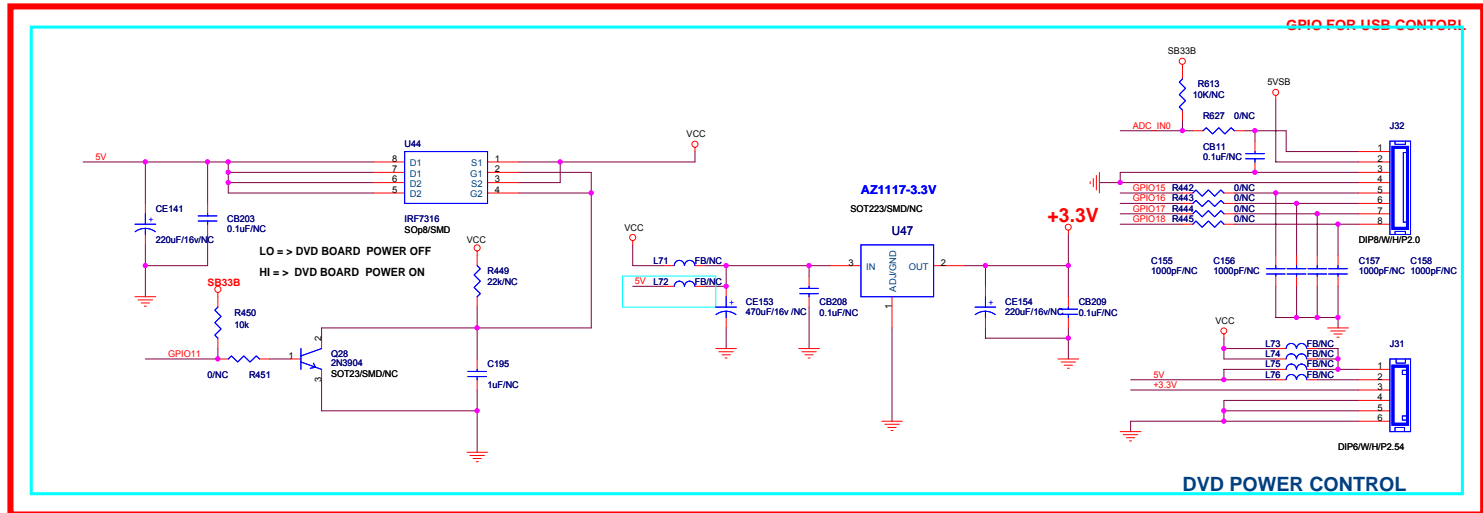
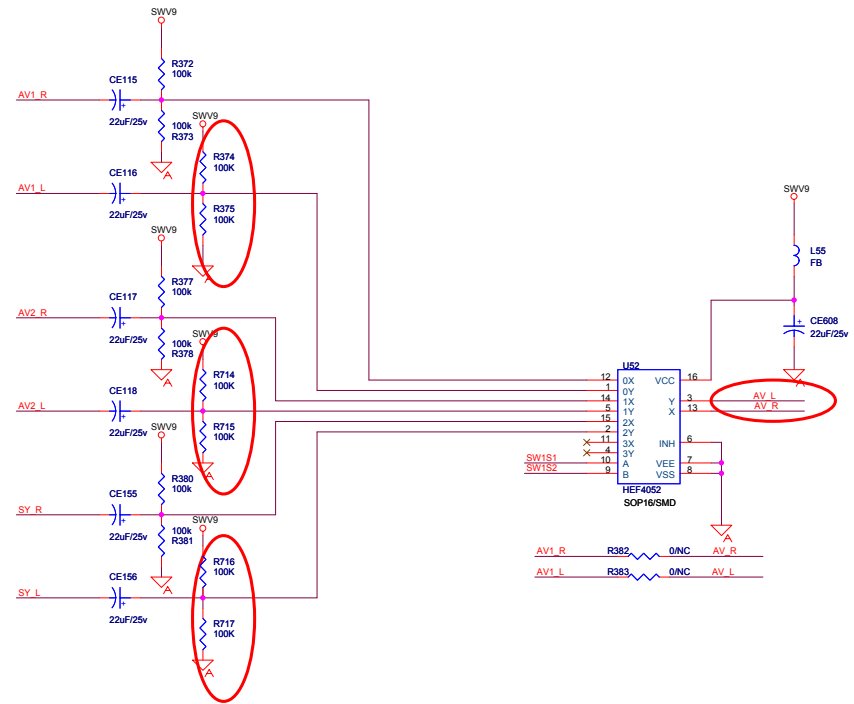
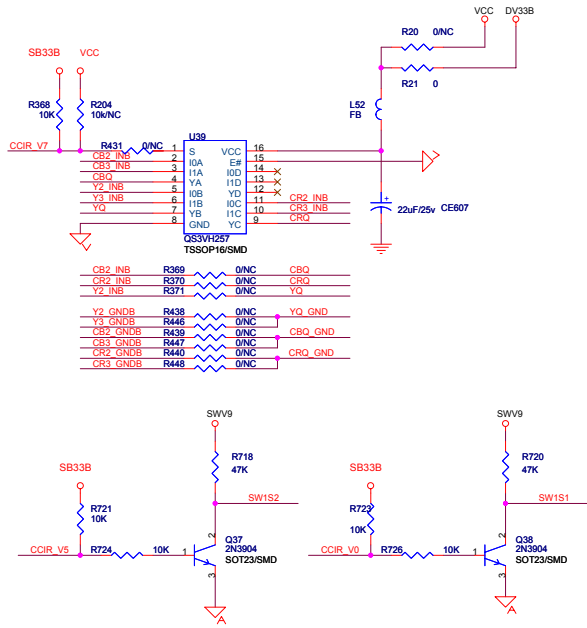
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Size	Document Number	<Designer>	Rev
B	AKAL_MT8202_27US_LVDS_V0.0	Checked: <Checker>	1
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INPUT

ADC_IN0	ADC_IN0	3
CCIR_V0	CCIR_V0	3
CCIR_V5	CCIR_V5	3
CCIR_V7	CCIR_V7	3
GPIO11	GPIO11	3
GPIO15	GPIO15	3
GPIO16	GPIO16	3
GPIO17	GPIO17	3
GPIO18	GPIO18	3
VFE_GND	VFE_GND	2,3,4,11
AADC_VSS	AADC_VSS	3,4,10
AV1_R	AV1_R	15
AV2_R	AV1_L	15
AV2_L	AV2_R	15
SY_R	AV2_L	15
SY_L	SY_R	15
YZ_INB	SY_L	15
YZ_GNDB	YZ_INB	15
CB2_INB	YZ_GNDB	10,15
CR2_INB	CB2_INB	15
CR2_GNDB	CR2_INB	10,15
Y3_INB	CR2_GNDB	10,15
Y3_GNDB	Y3_INB	15
CB3_INB	Y3_GNDB	15
CR3_INB	CB3_INB	15
CR3_GNDB	CR3_INB	15
9V	9V	1,7,9,14

OUTPUT

AV_R	AV_R	9
AV_L	AV_L	9
YO	YO	10
CBO	CBO	10
CRO	CRO	10
YQ_GND	YQ_GND	10
CBO_GND	YQ_GND	10
CRO_GND	CRO_GND	10



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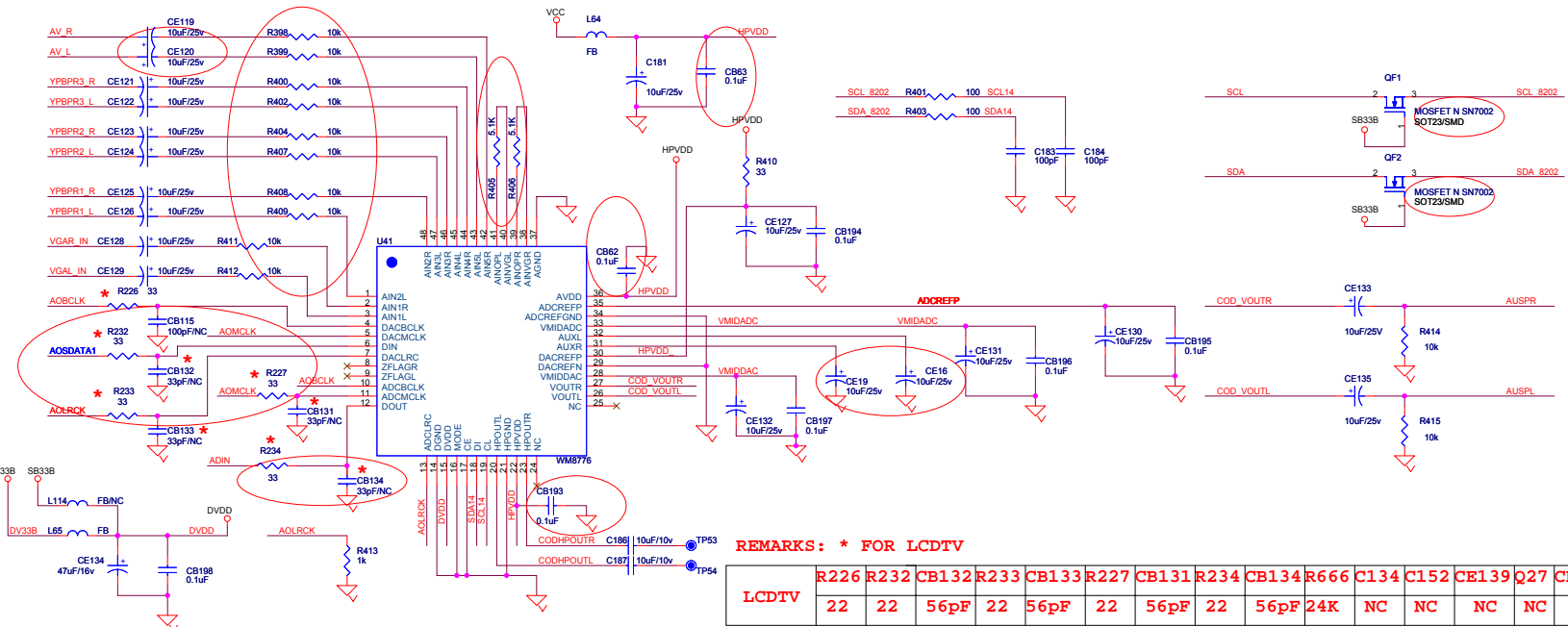
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DAUGHTER BOARD IN			
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INPUT

GPIO7	GPIO7	3
SCL	SCL	1,14
SDA_8202	SDA_8202	1,14
SCL_8202	SCL_8202	3,6,12
AOSDATA1	AOSDATA1	3
AOMCLK	AOMCLK	3,16
AOBCLK	AOBCLK	3,16
AOLRCK	AOLRCK	3,16
ADIN	ADIN	3,16
AV_L	AV_L	8
YBPBR1_L	YBPBR1_L	15
YBPBR1_R	YBPBR1_R	15
YBPBR2_L	YBPBR2_L	15
YBPBR2_R	YBPBR2_R	15
YBPBR3_L	YBPBR3_L	15
YBPBR3_R	YBPBR3_R	15
VGAR_IN	VGAR_IN	11
VGAR_OUT	VGAR_OUT	11
TESTP2	TESTP2	3
AR	AR	3
MU	MU	16
A_MUTE	A_MUTE	17
9V	9V	1,7,14

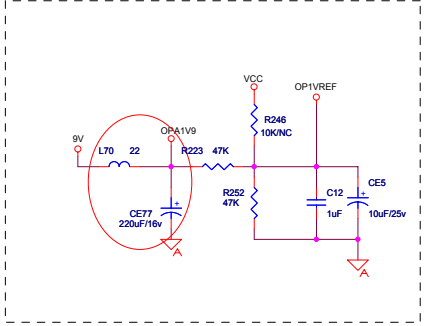
OUTPUT

AUSPR	AUSPR	16
AUSPL	AUSPL	16
AVL_OUT	AVR_OUT	16
AVL_OUT	AVR_OUT	16
CVBS_OUT	CVBS_OUT	6,15

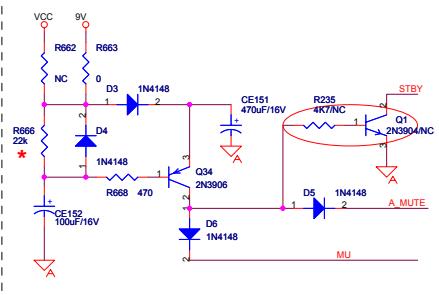
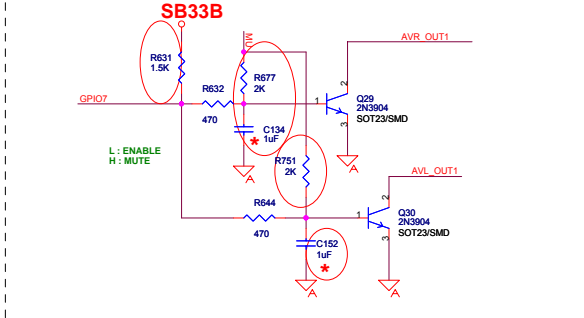


REMARKS: * FOR LCDTV

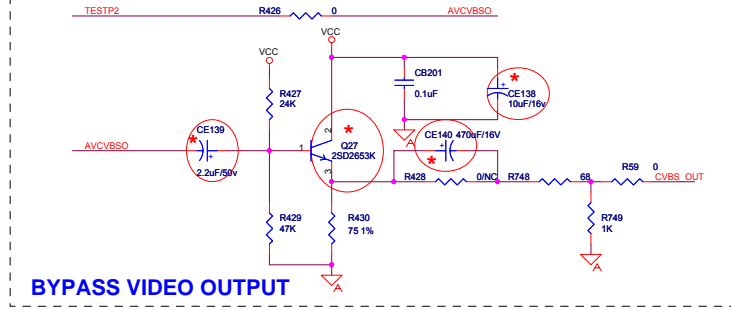
LCDTV	R226	R232	CB132	R233	CB133	R227	CB131	R234	CB134	R666	C134	C152	CE139	Q27	CE140	CE138
	22	22	56pF	22	56pF	22	56pF	22	56pF	24K	NC	NC	NC	NC	NC	NC



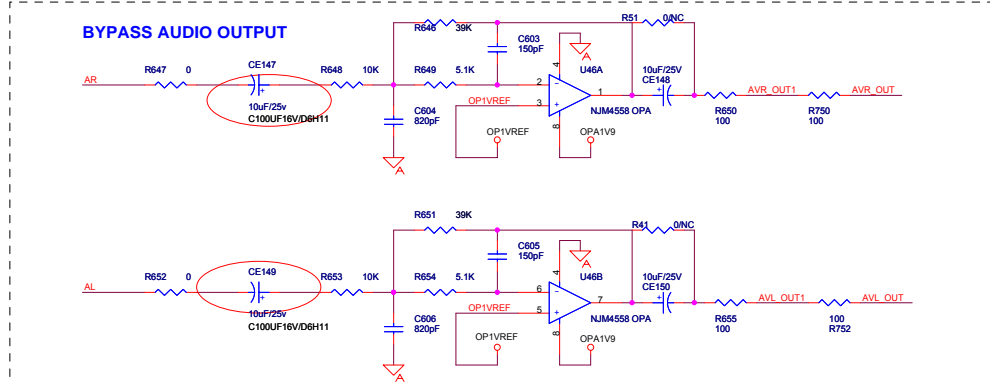
AUDIO BYPASS MUTE



BYPASS VIDEO OUTPUT



BYPASS AUDIO OUTPUT



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Title			
M8776 & VIDEO BYPASS			
Size	Document Number	AKAI_MIT8202_2TUS_LVDS_V0.0	Rev 1
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CVBS0 >>> CVBS0 3
 CVBS1 >>> CVBS1 3
 CVBS2 >>> CVBS2 3

SY0 >>> SY0 3
 SC0 >>> SC0 3

SY1 >>> SY1 3
 SC1 >>> SC1 3

Y0+ >>> Y0+ 3
 Y0- >>> Y0- 3
 PB0+ >>> PB0+ 3
 PB0- >>> PB0- 3
 PR0+ >>> PR0+ 3
 PR0- >>> PR0- 3
 SOY0 >>> SOY0 3

Y1+ >>> Y1+ 3
 Y1- >>> Y1- 3
 PB1+ >>> PB1+ 3
 PB1- >>> PB1- 3
 PR1+ >>> PR1+ 3
 PR1- >>> PR1- 3
 SOY1 >>> SOY1 3

MPX1 >>> MPX1 3
 MPX2 >>> MPX2 3

TO MT8202

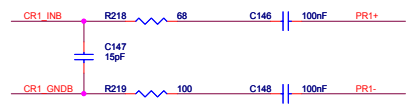
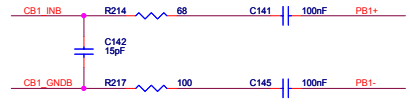
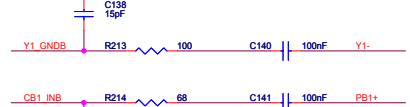
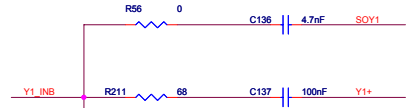
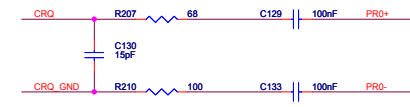
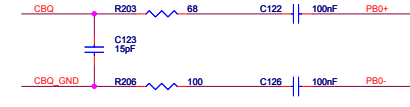
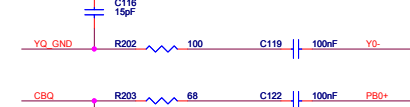
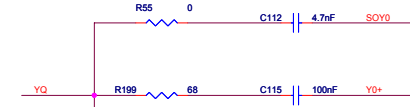
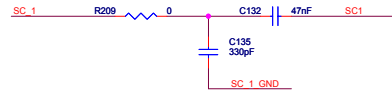
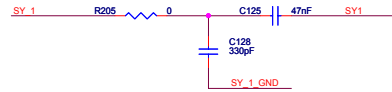
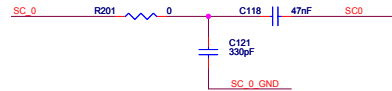
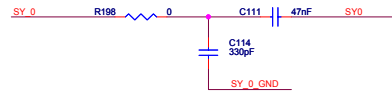
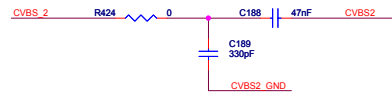
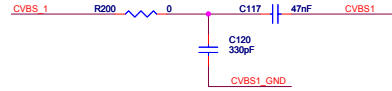
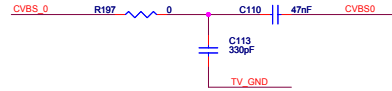
TV_GND >>> TV_GND 14
 CVBS_0 >>> CVBS_0 14
 SIF >>> SIF 14
 AF >>> AF 14
 CVBS_1 >>> CVBS_1 15
 CVBS1_GND >>> CVBS1_GND 15
 CVBS_2 >>> CVBS_2 15
 CVBS2_GND >>> CVBS2_GND 15
 SY_1 >>> SY_1 15
 SY_1_GND >>> SY_1_GND 15
 SC_1 >>> SC_1 15
 SC_1_GND >>> SC_1_GND 15
 SY_0 >>> SY_0 15
 SY_0_GND >>> SY_0_GND 15
 SC_0 >>> SC_0 15
 SC_0_GND >>> SC_0_GND 15

SOY1 >>> SOY1 3
 SOY0 >>> SOY0 3
 Y1_INB >>> Y1_INB 15
 Y1_GNDB >>> Y1_GNDB 8,15
 CR1_INB >>> CR1_INB 15
 CR1_GNDB >>> CR1_GNDB 8,15
 CB1_INB >>> CB1_INB 15
 CB1_GNDB >>> CB1_GNDB 8,15
 CRO >>> CRO 8
 YQ >>> YQ 8
 YQ_GND >>> YQ_GND 8
 CRO_GND >>> CRO_GND 8
 CRQ_GND >>> CRQ_GND 8

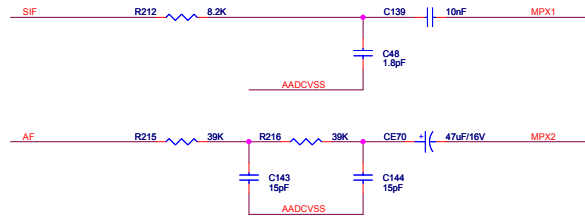
FROM AV BOARD

AADCSS >>> AADCSS 3,4

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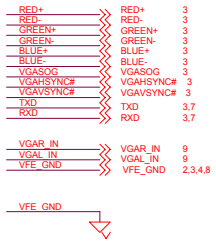


FROM Tuner

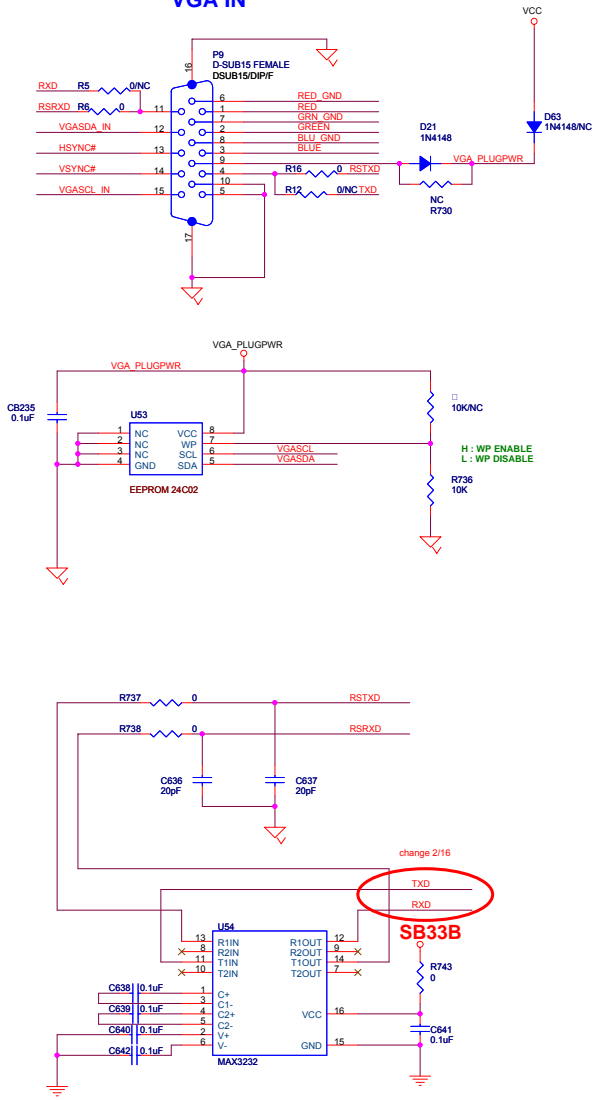


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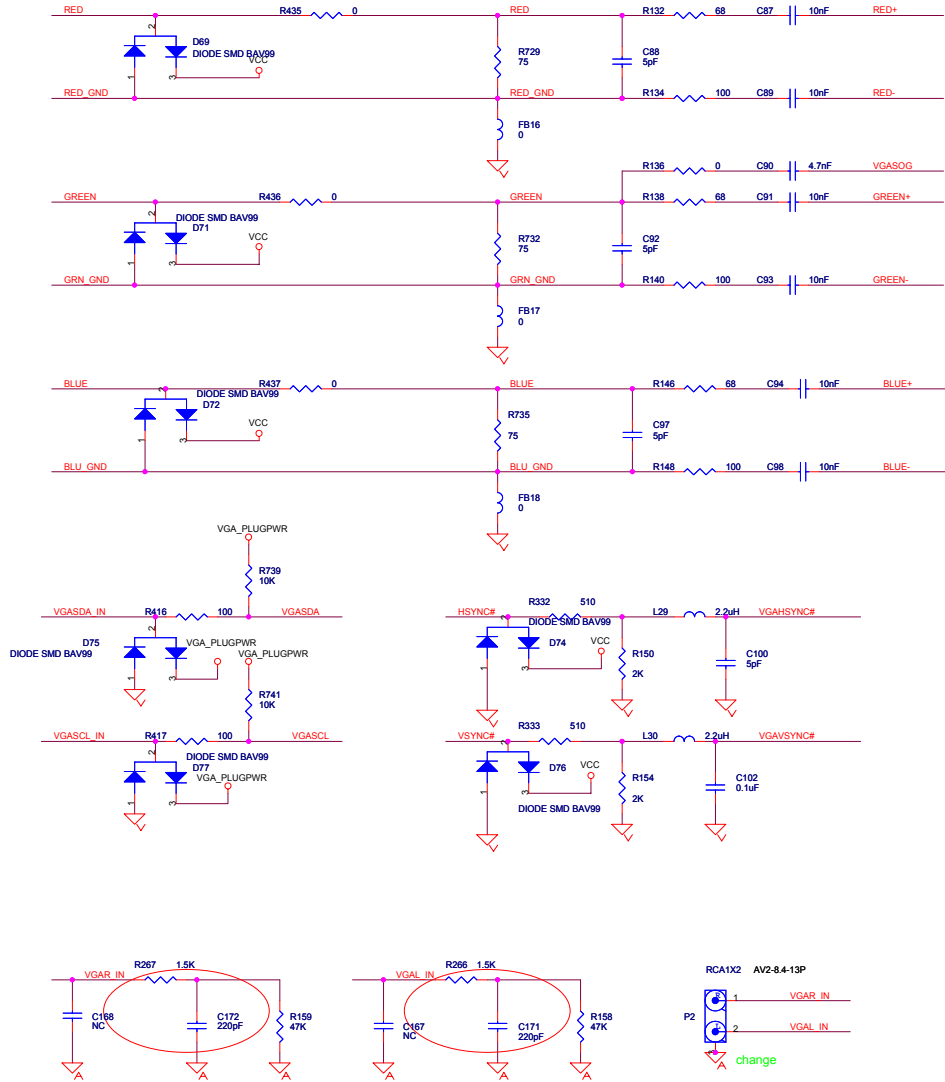
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VGA IN

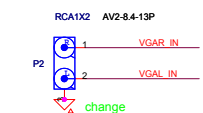


NEARLY VGA CON



NEARLY 8202

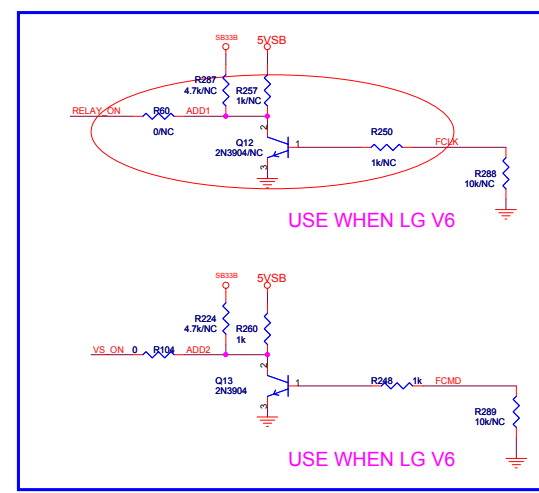
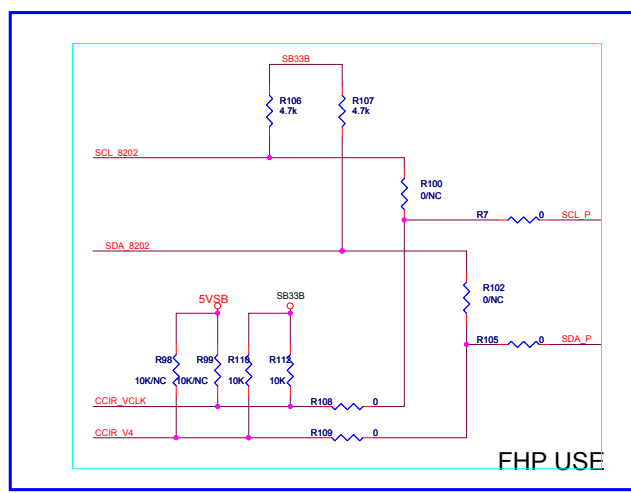
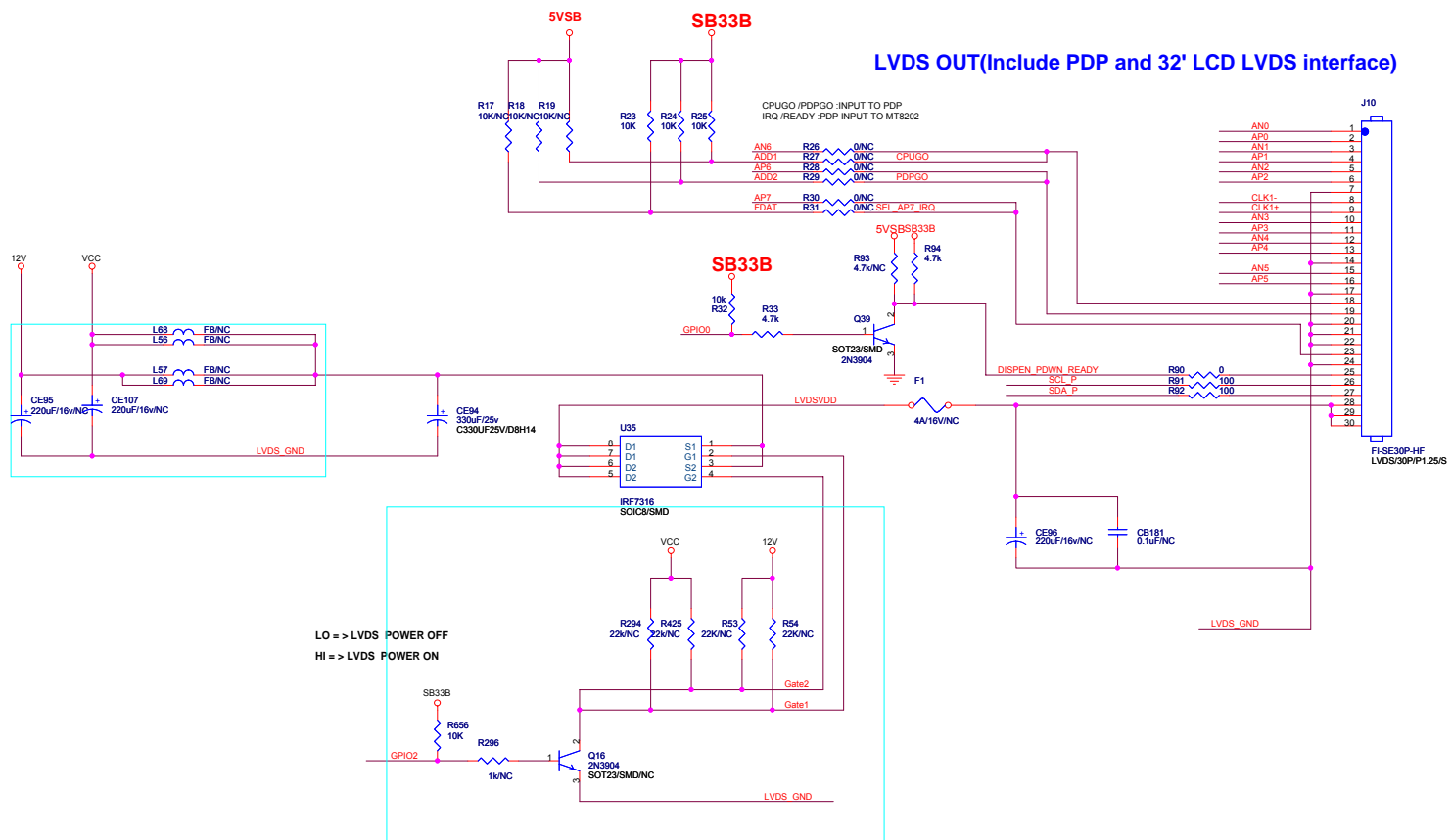
VGA/DVI AUDIO INPUT



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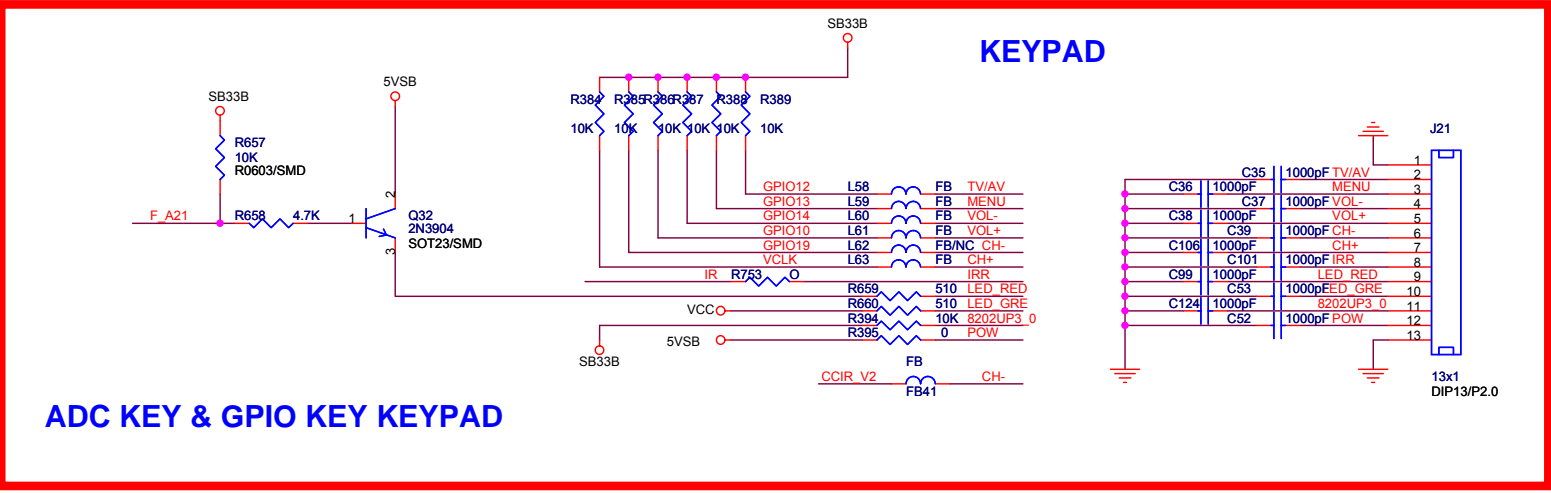
GPIO0	>>	GPIO2	3
CLK1+	>>	CLK1+	3
CLK1-	>>	CLK1-	4
AP0_7	>>	AP0_7	3
AND_6	>>	AND_6	3
LVDS_GND	>>	LVDS_GND	2,3,4
LVDS03	>>	LVDS03	2,3,4
CCIR_VCLK	>>	CCIR_VCLK	3
CCIR_V4	>>	CCIR_V4	3
FCLK	>>	FCMD	3
FCMD	>>	FCMD	3
FDAT	>>	FDAT	3
SCL_8202	>>	SCL_8202	3,6,9
SDA_8202	>>	SDA_8202	3,6,9
RELAY_ON	>>	RELAY_ON	1
VS_ON	>>	VS_ON	1
12V	>>	12V	1,13



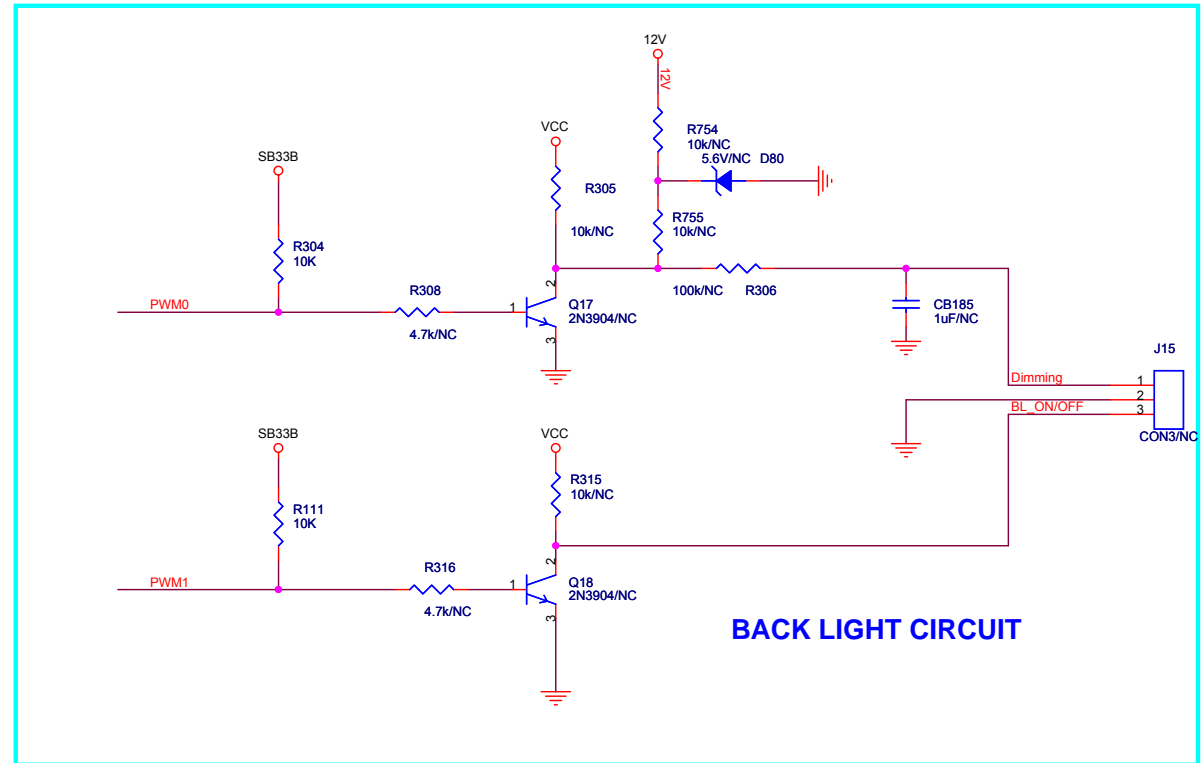
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LVDS OUT			
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Date:	Thursday, April 13, 2006	Sheet	17

IR	>>>IR	3,15
GPIO10	>>>GPIO10	3
GPIO12	>>>GPIO12	3
GPIO13	>>>GPIO13	3
GPIO14	>>>GPIO14	1,3
PWM0	>>>PWM0	3
PWM1	>>>PWM1	3
8202UP3_0	>>>8202UP3_0	3
GPIO14	>>>GPIO14	1,3
GPIO19	>>>GPIO19	1,3
VCLK	>>>VCLK	3
F_A21	>>>F_A21	3
CCIR_V2	>>>CCIR_V2	3
12V	>>>12V	1,12



ADC KEY & GPIO KEY KEYPAD



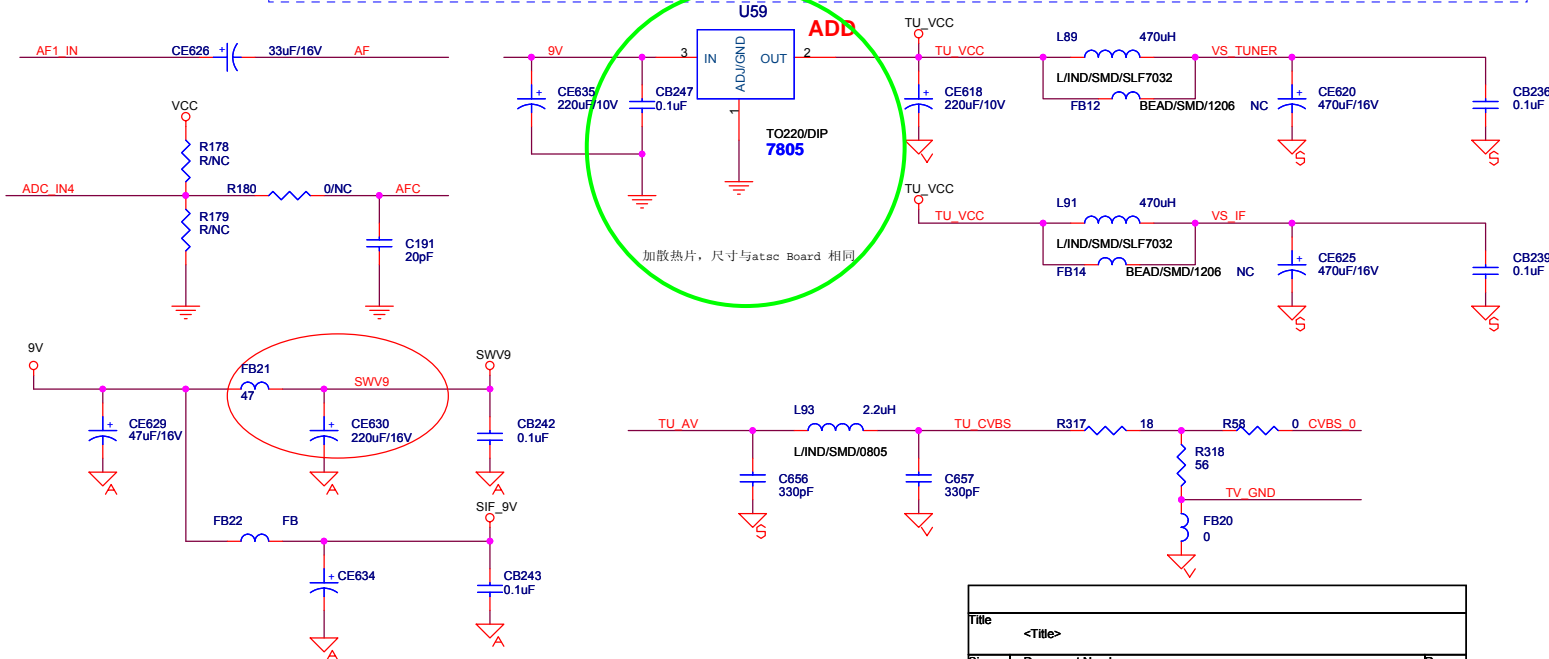
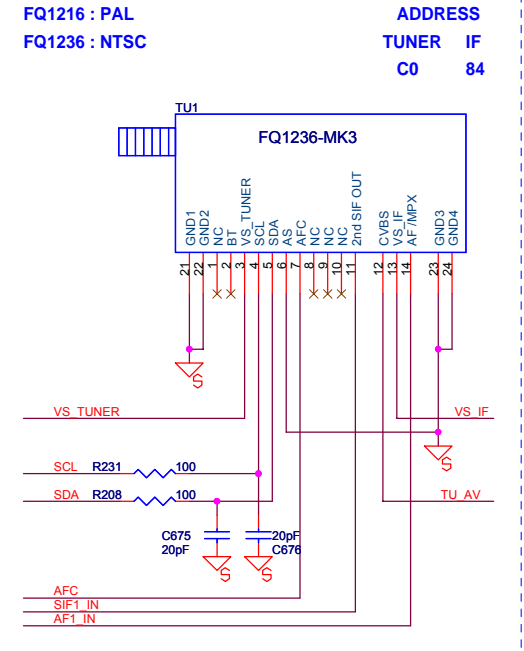
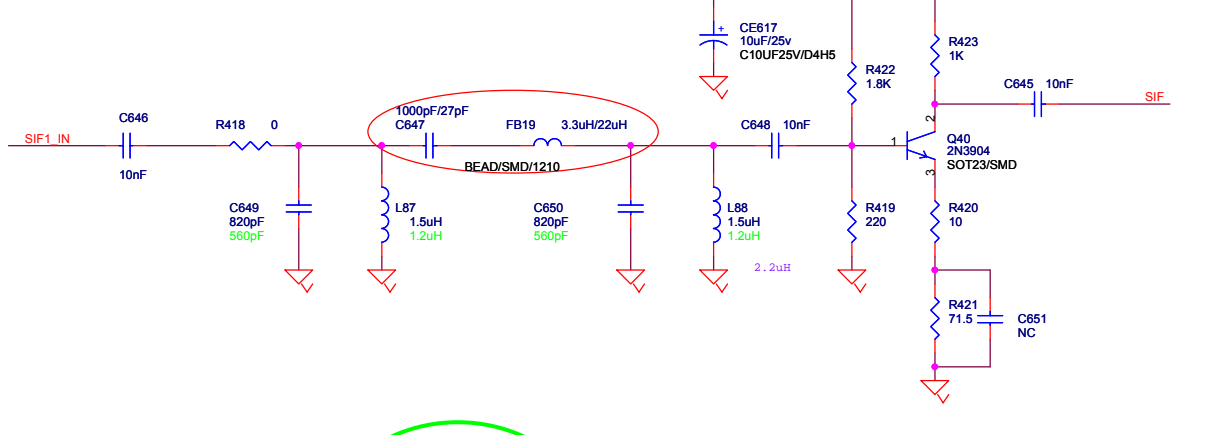
BACK LIGHT CIRCUIT

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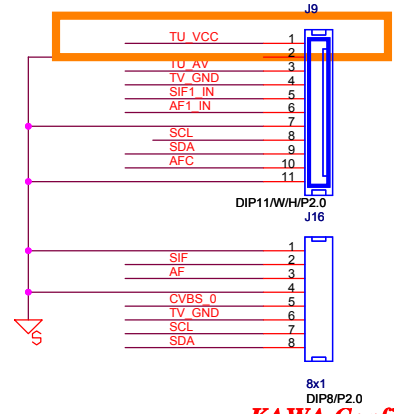
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SCL	SCL	1,9
SDA	SDA	1,9
CVBS_0	CVBS_0	10
TV_GND	TV_GND	10
AF	AF	10
SIF	SIF	10
ADC_IN4	ADC_IN4	3
9V	9V	1,7,9

TUNER SIF1NTSC 4.5MHz BPF



加散热片，尺寸与atse Board 相同

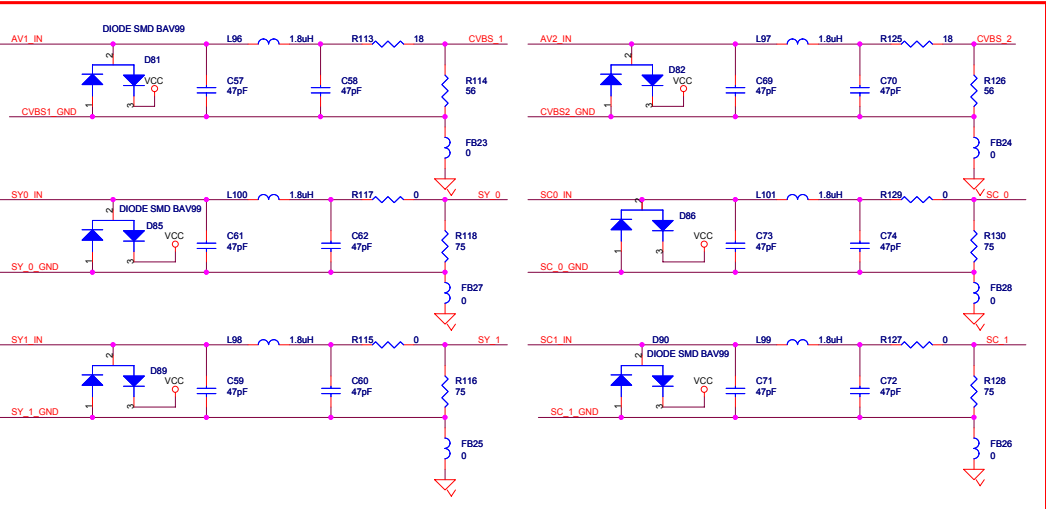
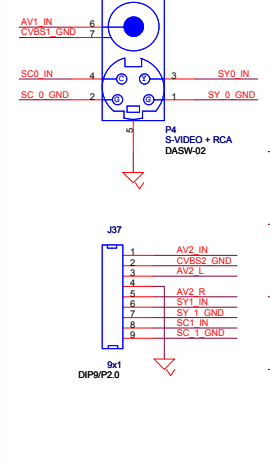


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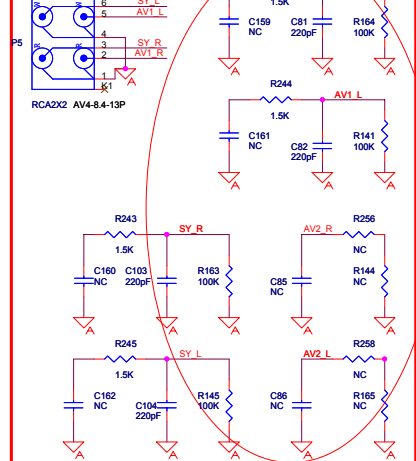
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Custom	<Doc>
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Rev	<Rev Code>

Title	TUNER IN		
Size	Document Number	<Designer>	Rev
Custom	KAWA_MT8202_27US_LVDS_V0.0	Checked: <Checker>	1
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AV /YC VIDEO IN

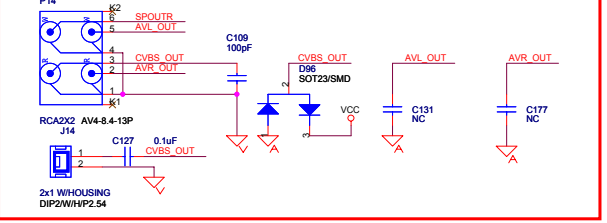


AV /YC AUDIO IN

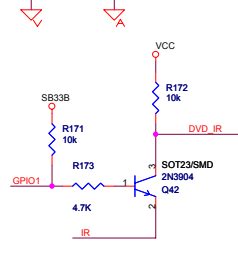
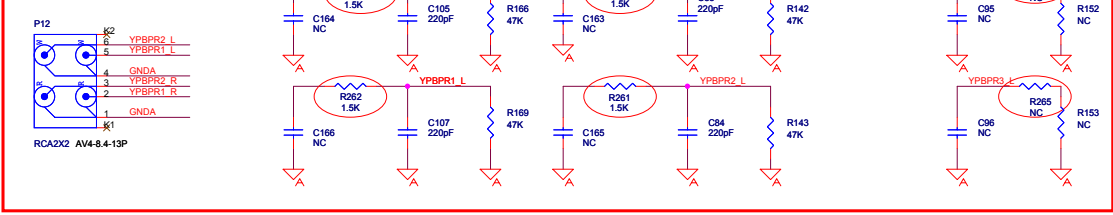


GPIO1 IR	GPIO1 IR	3
SY 1	SY_1	10
SY 1 GND	SY_1_GND	10
SC 1 GND	SC_1_GND	10
SY 0	SY_0	10
SY 0 GND	SY_0_GND	10
SC 0 GND	SC_0_GND	10
CVBS1 GND	CVBS1_GND	10
CVBS2 GND	CVBS2_GND	10
SPOUTR	SPOUTR	16
AVR_OUT	AVR_OUT	9
AVL_OUT	AVL_OUT	9
CVBS_OUT	CVBS_OUT	6.9
AV1_R	AV1_R	8
AV1_L	AV1_L	8
AV2_R	AV2_R	8
AV2_L	AV2_L	8
SY_R	SY_R	8
SY_L	SY_L	8
YPBPR1_L	YPBPR1_L	8
YPBPR1_R	YPBPR1_R	8
YPBPR2_L	YPBPR2_L	9
YPBPR2_R	YPBPR2_R	9
YPBPR3_L	YPBPR3_L	9
YPBPR3_R	YPBPR3_R	9
Y1_INB	Y1_INB	8,10
Y1_GNDB	Y1_GNDB	8,10
C81_INB	C81_INB	8,10
C81_GNDB	C81_GNDB	8,10
C81_INB	C81_INB	8,10
C81_GNDB	C81_GNDB	8,10
Y2_INB	Y2_INB	8,10
Y2_GNDB	Y2_GNDB	8,10
C82_INB	C82_INB	8,10
C82_GNDB	C82_GNDB	8,10
Y3_INB	Y3_INB	8,10
Y3_GNDB	Y3_GNDB	8,10
C83_INB	C83_INB	8,10
C83_GNDB	C83_GNDB	8,10
CR3_INB	CR3_INB	8,10
CR3_GNDB	CR3_GNDB	8,10
GNDV	GNDV	
GNDV	GNDV	

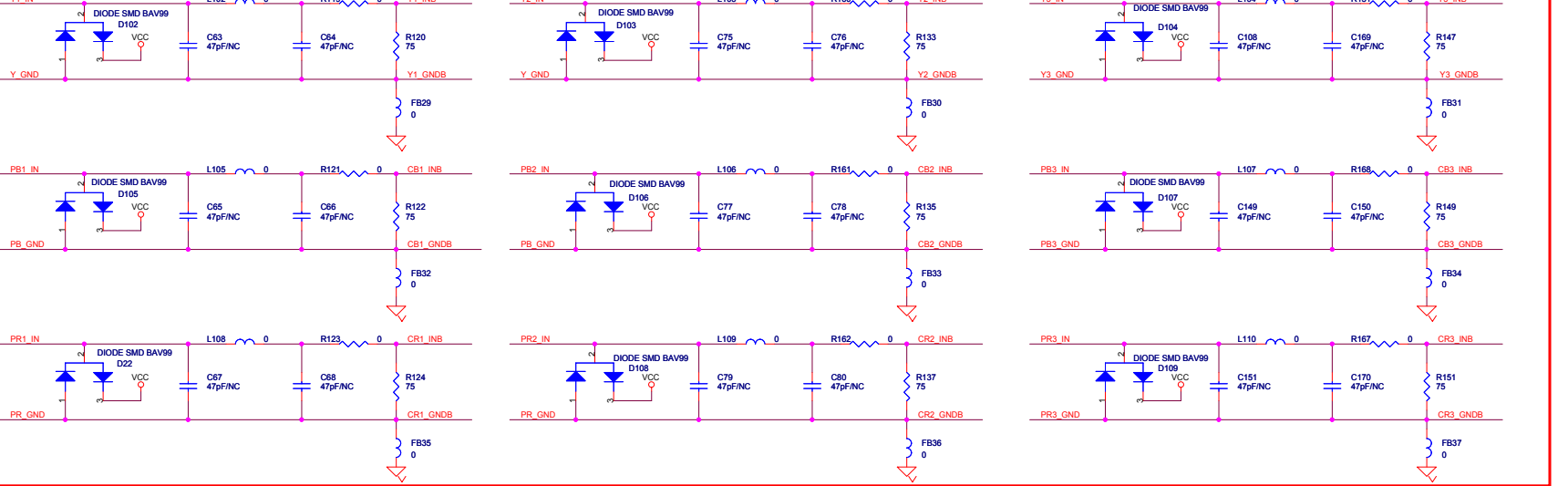
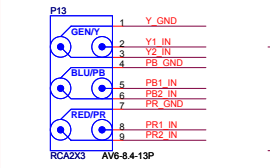
AV VIDEO/AUDIO OUT.



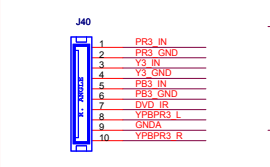
YPBPR AUDIO IN.



YPBPR VIDEO IN.



YPBPR1 / 2 INPUT.

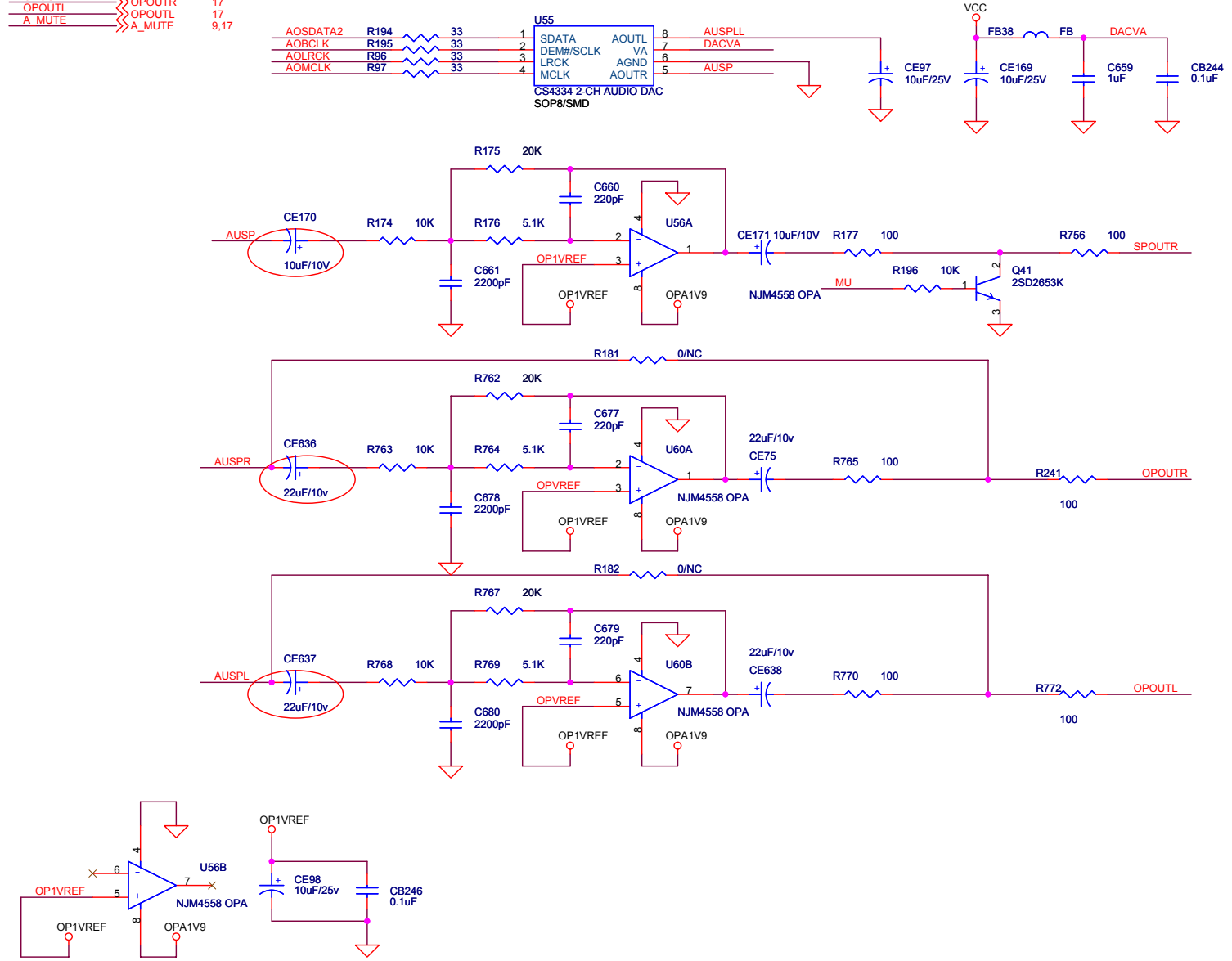


YPBPR 3 INPUT.

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AOSDATA2 >>> AOSDATA2 3
 AOMCLK >>> AOMCLK 3,9
 AOBCLK >>> AOBCLK 3,9
 AOLRCK >>> AOLRCK 3,9
 MU >>> MU 9
 SPOUTR >>> SPOUTR 15
 AUSPR >>> AUSPR 9
 AUSPL >>> AUSPL 9
 OPOUTL >>> OPOUTL 17
 OPOUTR >>> OPOUTR 17
 A_MUTE >>> A_MUTE 9,17



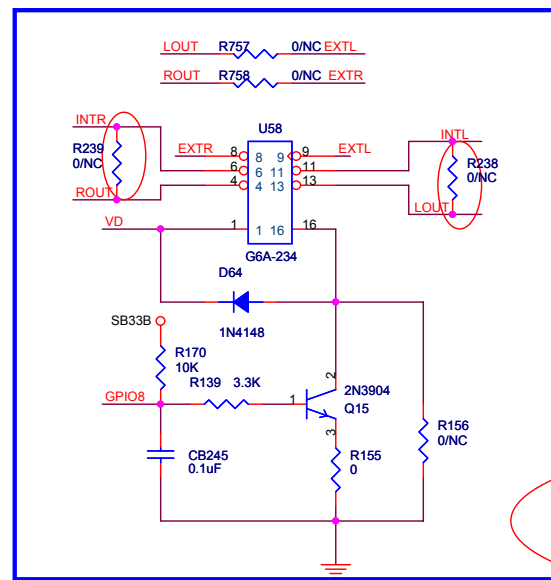
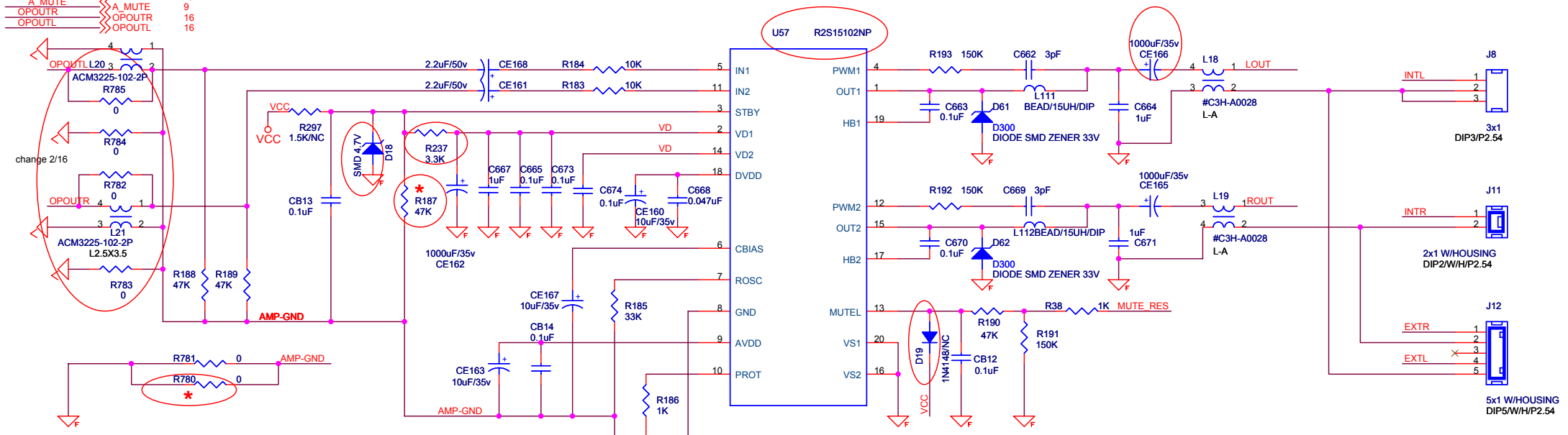
GPIO DECRPTION

- UP3_4 : SW SCL
- UP3_5 : SW SDA
- ERO0/UP3_0 :KEYPAD POWER
- ERO1/UP3_1 : MAIN POWER SWITCH
- VCLK : KEPAD CH+
- GPIO19 : KEPAD CH-
- DE/GPIO : DVD IR
- CCIR_CLK : PDP USE
- CCIR_V4 : PDP USE
- GPIO0 : PDP USE
- GPIO1 : NO USE
- GPIO2 : LVDS POWER SW
- GPIO3 : DTV POWER CONTROL
- GPIO4 : EEPROM WRITE PROTECT
- GPIO5/TXD : 2nd UART FOR MT5351
- GPIO6/RXD : 2nd UART FOR MT5351
- GPIO7 : AUDIO BYPASS MUTE CONTROL
- GPIO8 : SPEAKER SWITCH
- GPIO9 : AUDIO MUTE
- GPIO10 : Indicates active video at HDMI port
- GPIO11 : DVD POWER CONTROL
- GPIO12 : AV SWITCH
- GPIO13 : HDMI Hot Plug Detect
- GPIO14 : NO USE
- GPIO[15..18] : FOR DVD CONTROL
- GPIO/PWM0 : DIMMING
- GPIO/PWM1 : BACKLIGHT ON/OFF
- OUT_27Mhz/GPIO : HDMI CRYSTAL
- SDA1 : TO MT5351 I/F REQUEST
- SCL1 : TO MT5351 I/F READY
- F_A21 : KEYPAD(LED RED)
- ADCIN0 : KEYPAD
- ADCIN3:PDP 5VD DETECT
- ADCIN4:FOR TUNER AFC
- CCIR_V[0-3] : KEYPAD
- CCIR_V5 : AUDIO SWITCH
- CCIR_V6 : RESET DTV
- CCIR_V7 : YBPBR VIDEO SWITCH

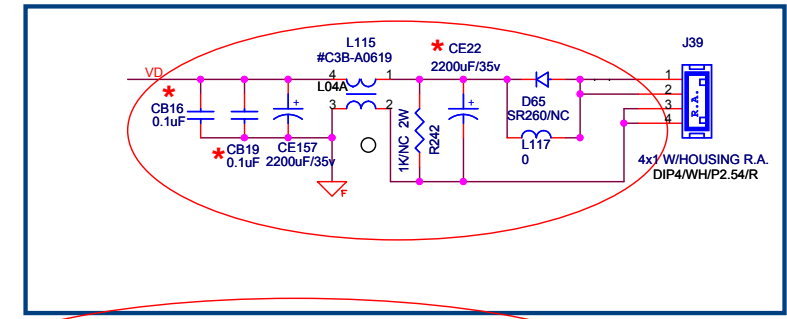
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GPIO8	GPIO8	3
GPIO9	GPIO9	3
AUSPR	AUSPR	9,16
AUSPL	AUSPL	9,16
A_MUTE	A_MUTE	9
OPOUTR	OPOUTR	16
OPOUTL	OPOUTL	16

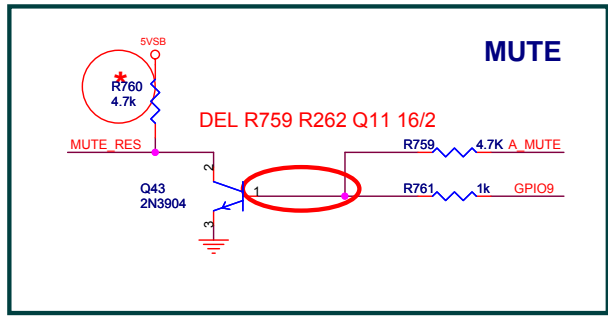


GPIO8: SPEAKER SWITCH (INTERNAL OR EXTERNAL)



REMARKS: * FOR LCDTV

LCDTV	R780	R187	R760	CB16	CB19	CE22
	NC	51K	2.2K	NC	NC	NC



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Title			
AUDIO Amplifier			
Size	Document Number	<Designer>	Rev
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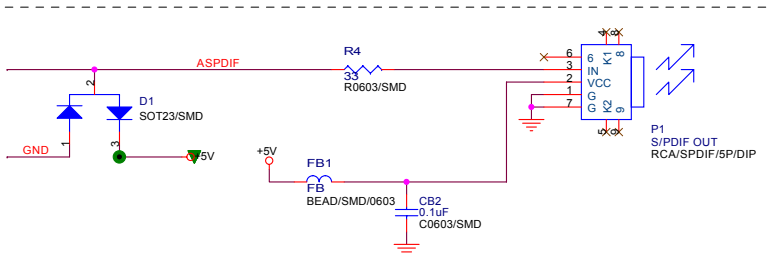
MT5111 / MT5351 REFERENCE DESIGN - 4 LAYERS

Rev	History	P#	DATE
RA-V1	INITIAL VERSION		2005/06/15
RA-V2	ADDED AUDIO SWITCH / REFINE POWER CIRCUIT		2005/07/14

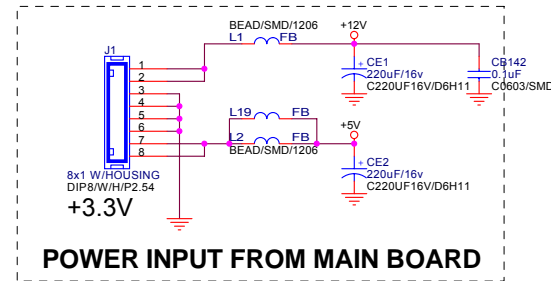
- 01. INDEX AND INTERFACE
- 02. POWER
- 03. TUNER
- 04. MT5111 ASIC
- 05. MT5351 ASIC
- 06. MT5351 PERIPHERAL
- 07. DDR MEMORY
- 08. NOR FLASH / JTAG / UART

NS : NON-STUFF

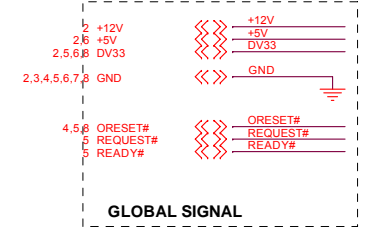
NAME	TYPE	DEVICE
+12V	POWER +12V	POWER SUPPLY
+5V	POWER +5V	POWER SUPPLY
+5V_tuner	POWER +5V	TUNER POWER
DV33_DM	POWER +3V3	MT5111 POWER
DV18	POWER +1V8	MT5111 POWER
DV33	POWER +3V3	MT5351 POWER
AV33	POWER +3V3	MT5351 ANALOG POWER
DV25	POWER +2V5	MT5351 DDR POWER
DV12	POWER +1V2	MT5351 POWER
GND	GROUND	GROUND



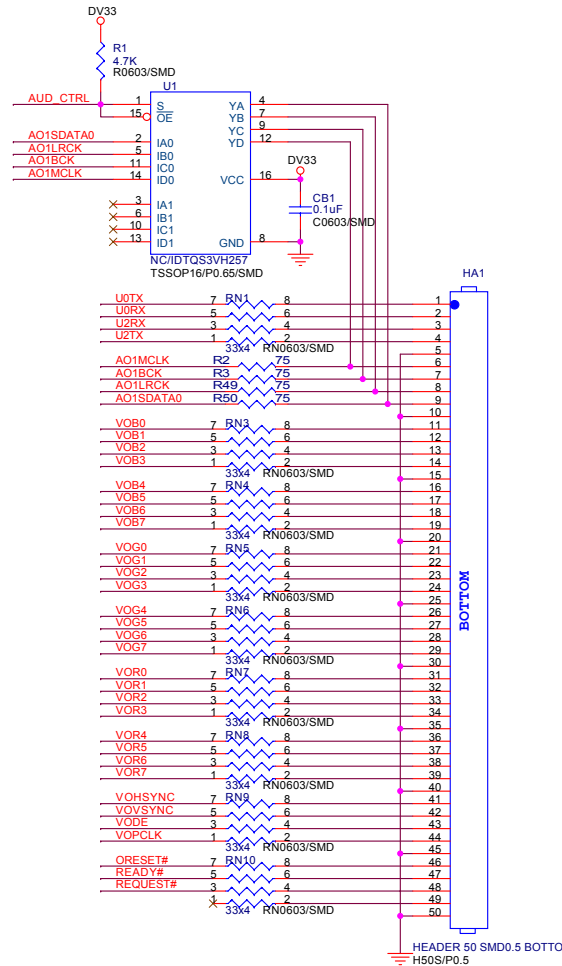
SPDIF CIRCUIT



POWER INPUT FROM MAIN BOARD



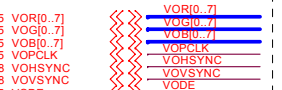
GLOBAL SIGNAL



DIGITAL OUTPUT



UART (RS232)



DIGITAL VIDEO OUTPUT



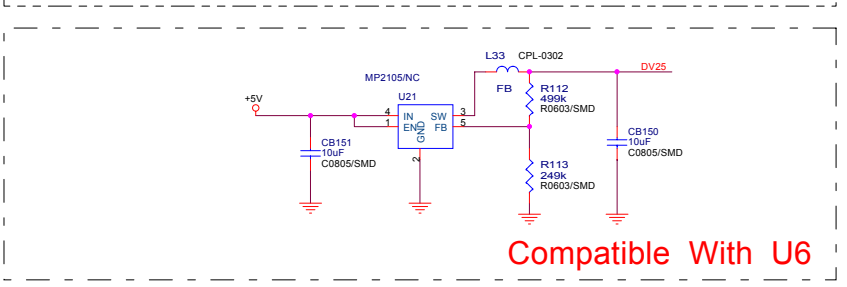
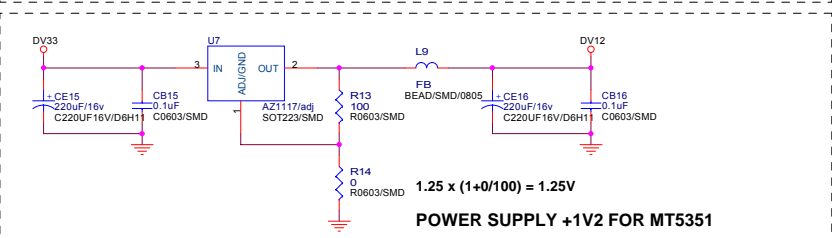
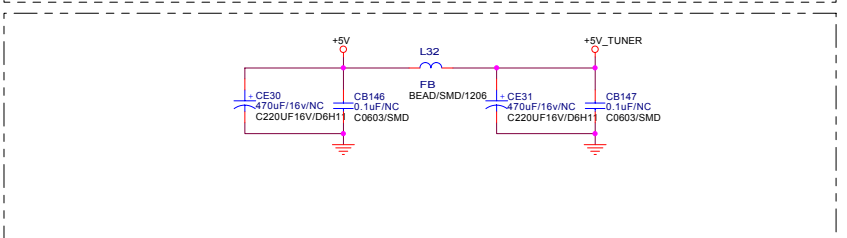
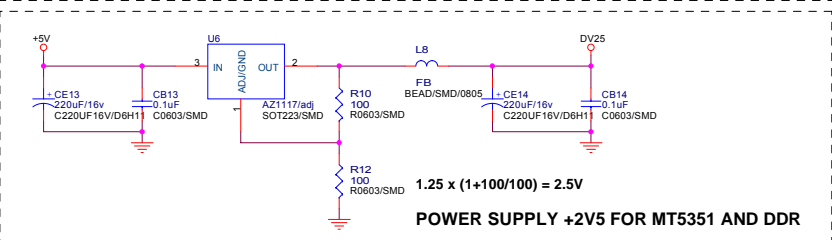
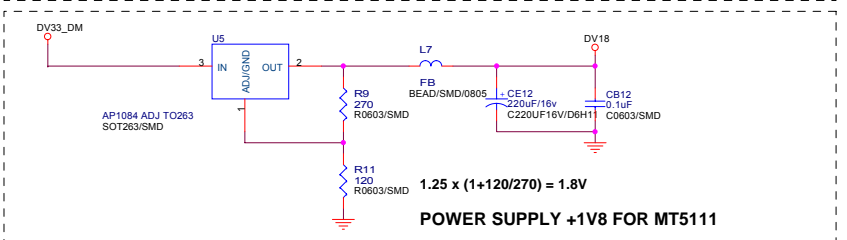
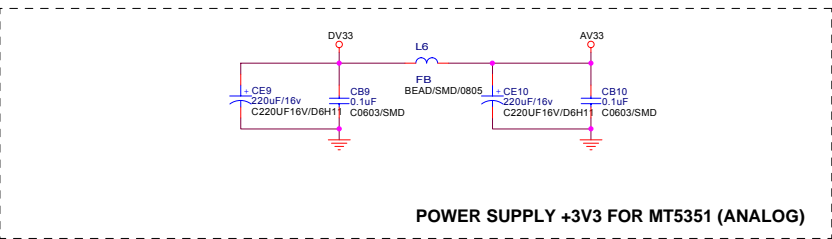
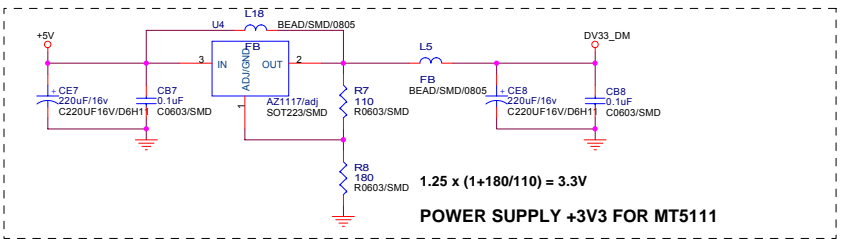
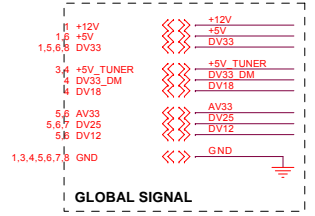
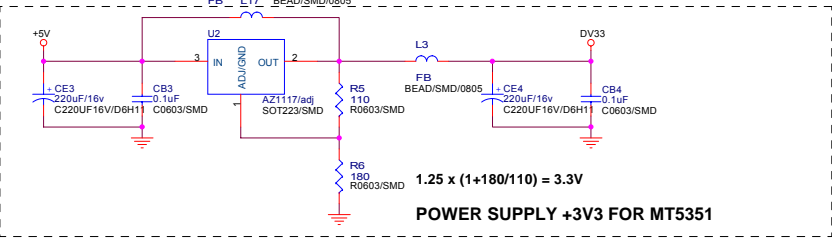
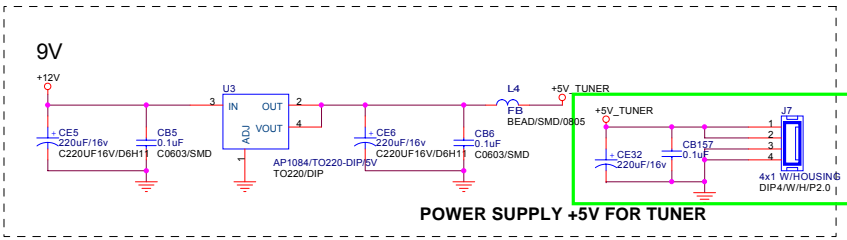
DIGITAL AUDIO INTERFACE



AUD_CTRL

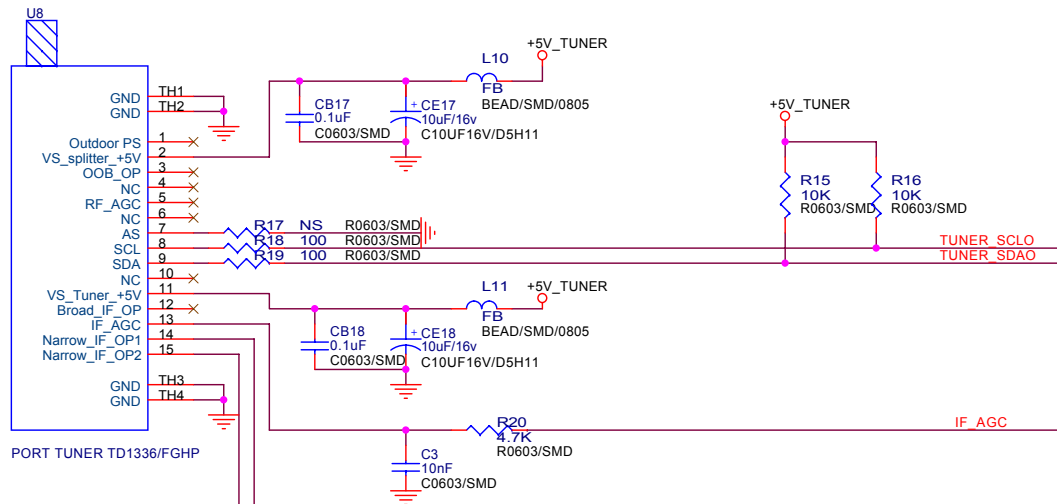
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Custom	MT5351RA-V2			1			
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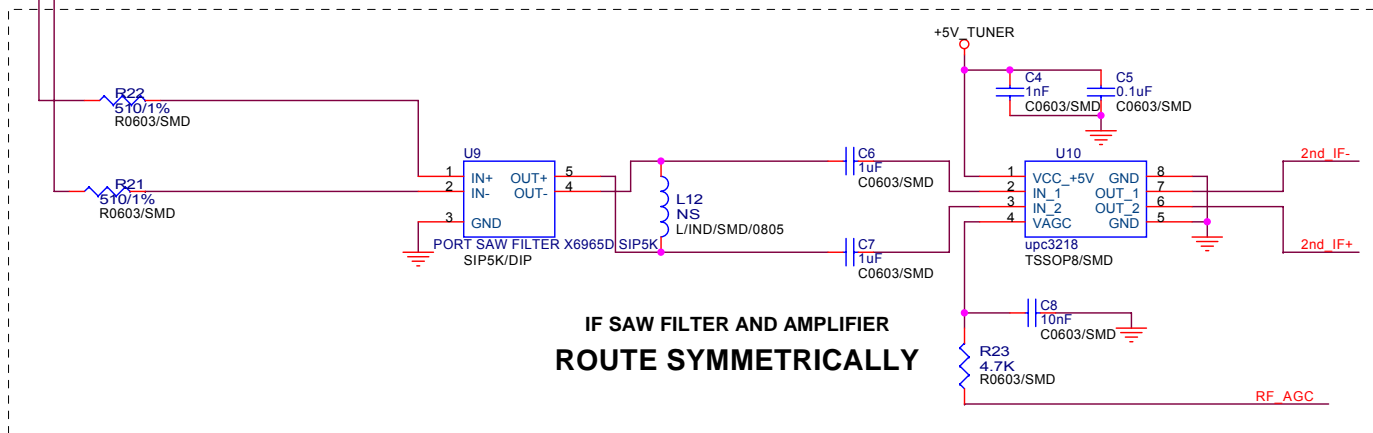


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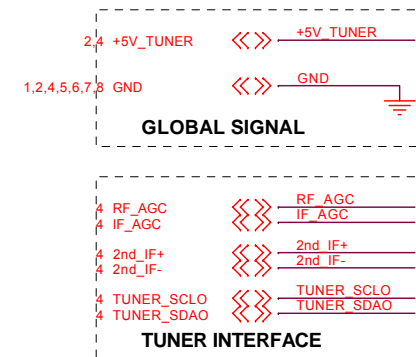
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PORT TUNER TD1336/FGHP

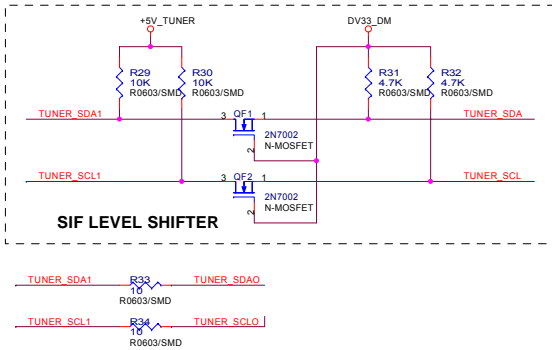
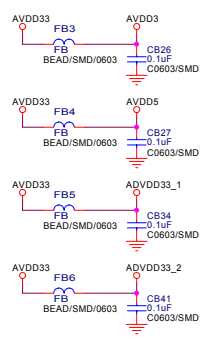
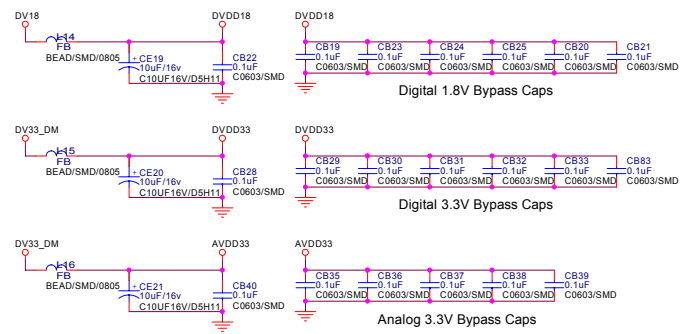
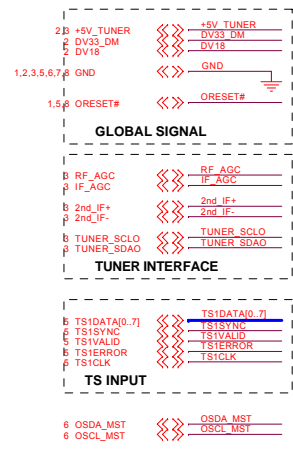
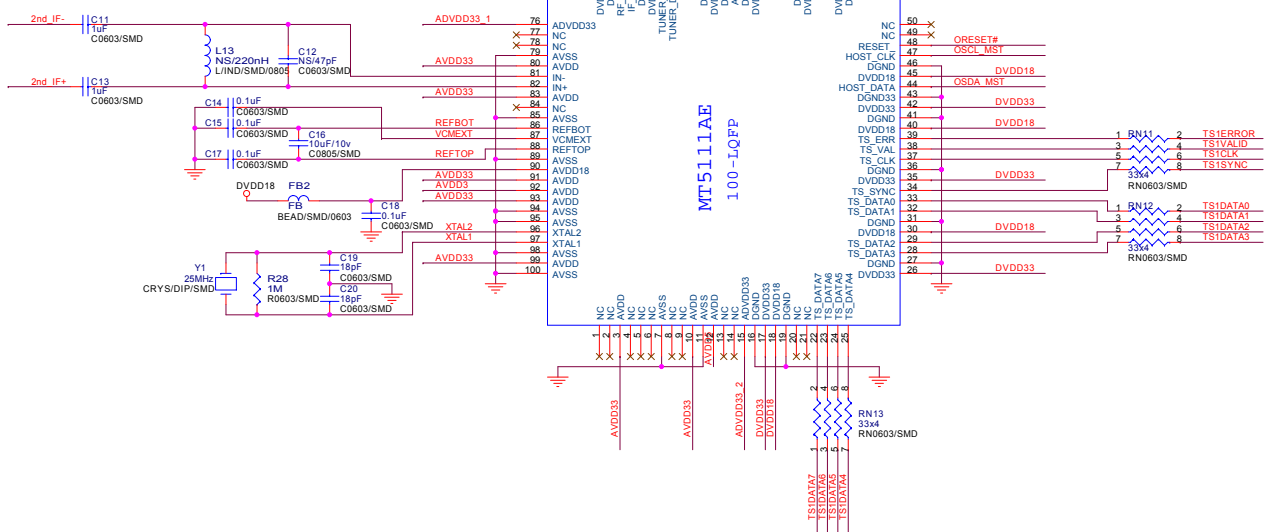
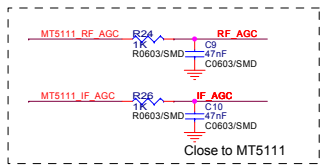


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ROUTE SYMMETRICALLY**



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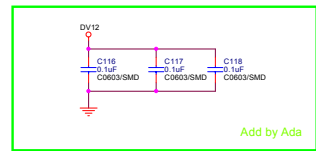
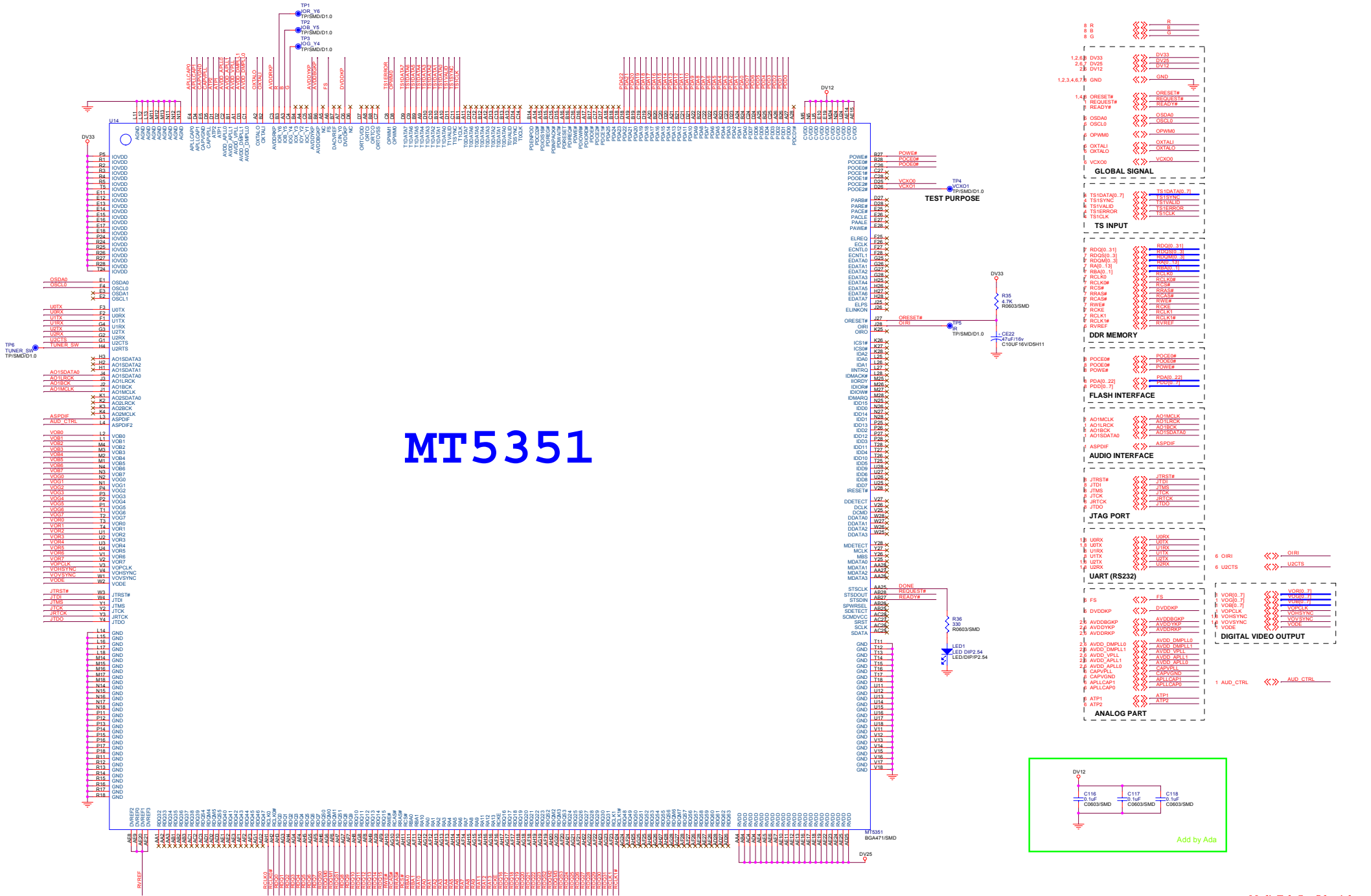
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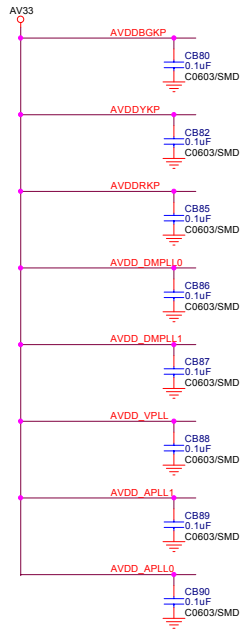
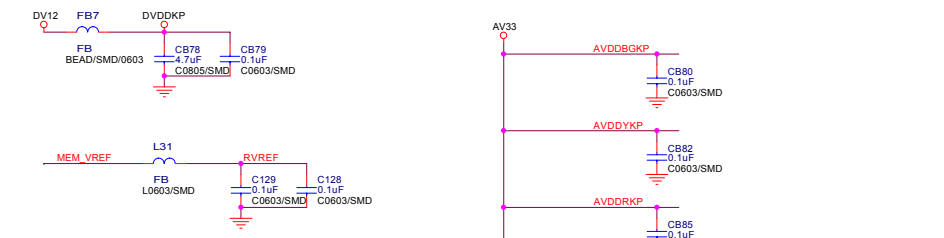
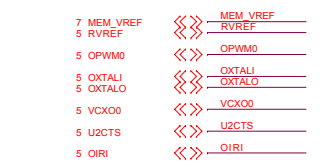
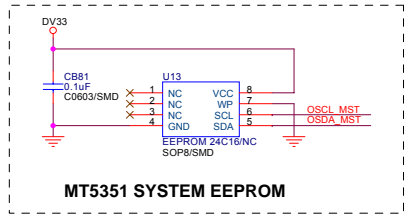
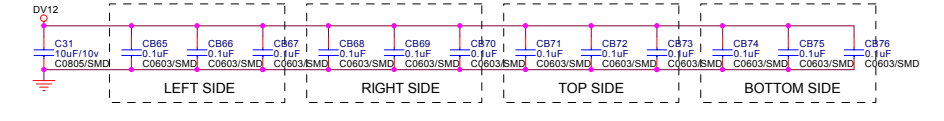
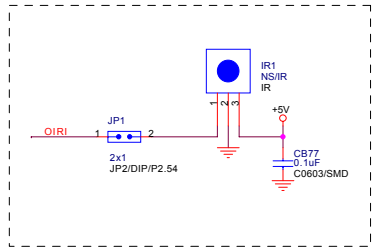
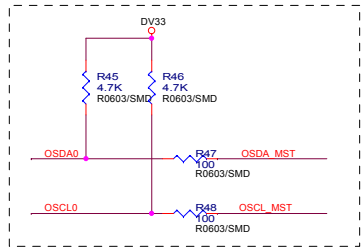
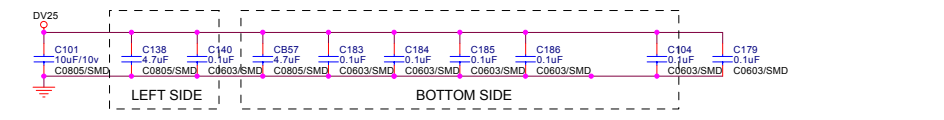
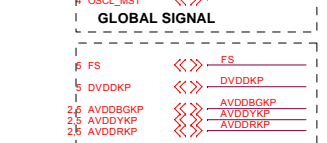
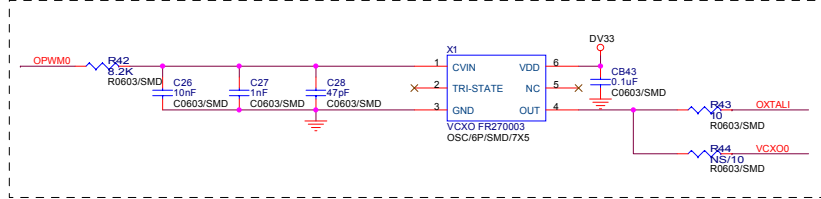
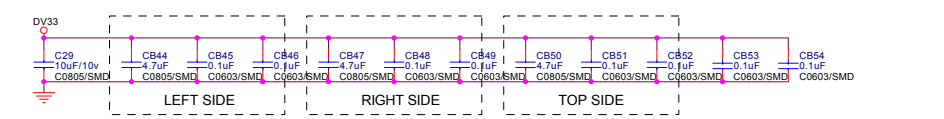
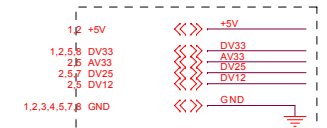
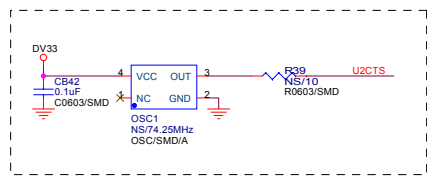
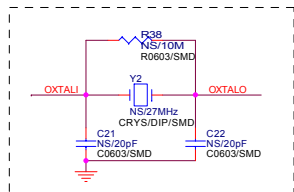
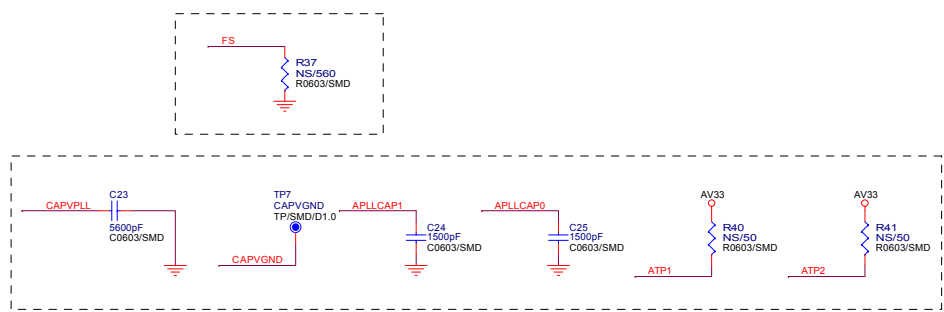
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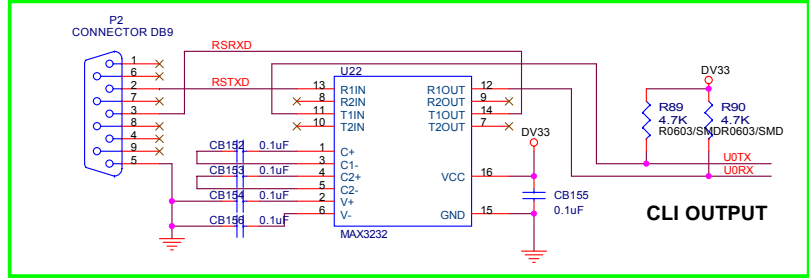
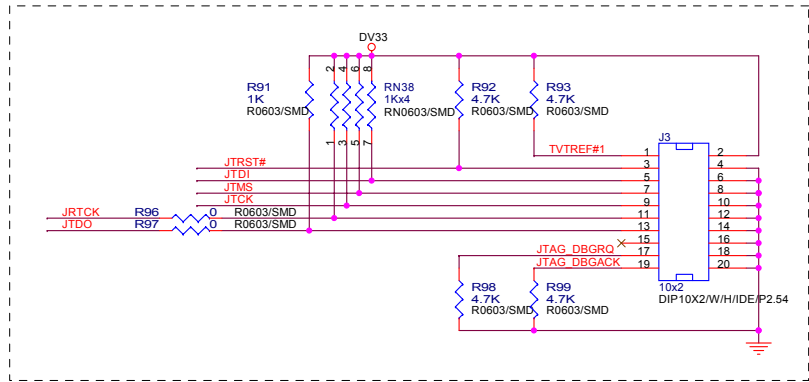
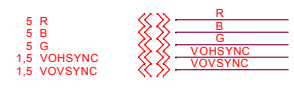
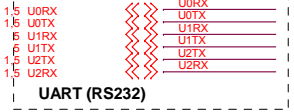
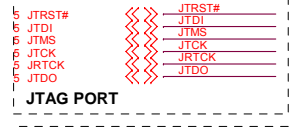
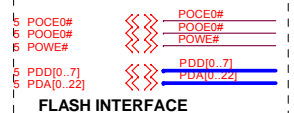
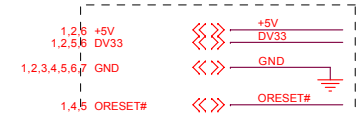
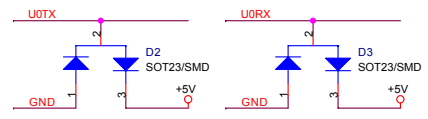
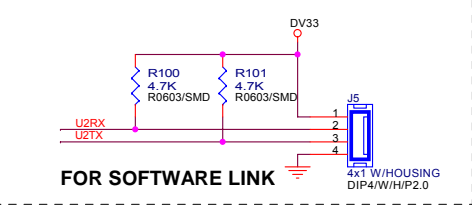
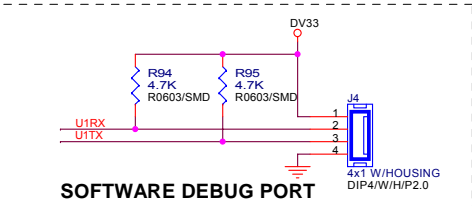
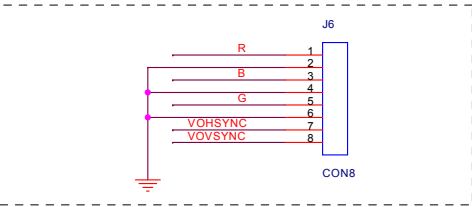
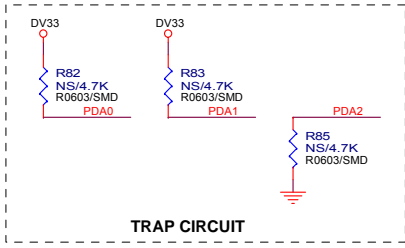
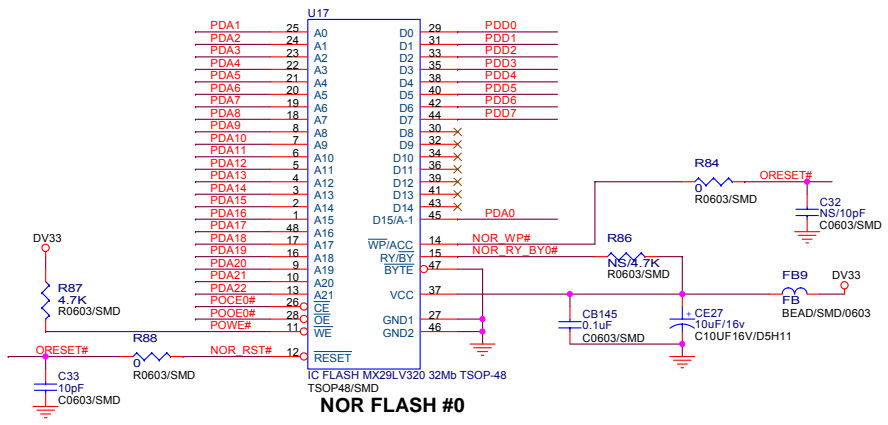
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File	MT5351 ASIC		
Size	Document Number	MT5351A-V2	Rev 1
Customer	TwinScan Chan		
Date	Monday, February 20, 2006	Sheet	8 of 8



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Title				MT5351 PERIPHERAL	
Size	Document Number	MT5351RA-V2		Rev	1
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Size Custom	Document Number MT5351RA-V2	TwinSon Chan	Rev 1
Date: Monday, February 20, 2006	Sheet 8	of 8	

Basic Operations & Circuit Description

MODULE

There are 1 pcs panel and 5 pcs PCB including 3 pcs Extension PCB, 1 pcs Timming controller board and 1 pcs Back Light board in the Module.

SET

There are 6 pcs PCBs including 1 pcs ATV Tuner board, 1 pcs keypad board, 1 pcs Remote Control Receiver board, 2 pcs L/R Speakers and 1 pcs Main(Video)board, 1 pcs ATSC board in the SET.

PCB funtion

1. Power :

(1). Input voltage: AC 120V, 60Hz.

(2). To provide power for PCBs.

2. Main board : To converter TV signals, S signals, AV signals, Y Pb/Cb Pr/Cr signals, DVI/HDMI signals and D-SUB signals to digital ones and to transmit to Control board.

3. Control board : Dealing with the digital signal for output to panel.

4. Extension board : Output addressing signals.

5. ATV Tuner Board : To convert TV RF signal to video and SIF audio signal to Main board.

6. ATSC Board : Receiver and converter ATSC TV signal to transmit to main board.

PCB failure analysis

1. CONTROL : a. Abnormal noise on screen. b. No picture.
2. MAIN :
 - a. Lacking color, Bad color scale.
 - b. No voice. (Make sure status: Mute / Internal, External speaker)
 - c. No picture but with signals output, OSD and back light.
 - d. Abnormal noise on screen.
3. POWER : NO picture, no power output.
4. Back Light :
 - a. No picture.
 - b. Flash on screen.
 - c. Darker picture with signals.
5. ATV Tuner :
 - a. No ATV Noise
 - b. No ATV signals
6. ATSC: a No ATSC TV signal

Main IC Specifications

- M13S128168A (ESMT)
2M x 16 Bit x 4 Banks Double Data Rate SDRAM
- MT5111CE
Single-Chip HDTV/CATV Demodulator
- MT5351
MT5351 is a DTV Backend Decoder SOC which support flexible transport demux, HD MPEG-2 video decoder, MPEG1,2, MP3, AC3 audio decoder, HDTV encoder. MT5351 is powered by ARM 926EJ with 16K I-Cache and 16K D-Cache. It can support 64Mb to 1Gb DDR DRAM devices with configurable 32/64 bit data bus interface.
- MT8202
MT8202G is a highly integrated Single-Chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals.
- MT8293
HDMI PanelLink Cinema Receiver
- R2S15102NP
Digital Power Amplifier R2S15102NP
- WM8776
24-bit, 192kHz Stereo CODEC with 5 Channel I/P Multiplexer

MT5111CE

Single-Chip HDTV/CATV Demodulator

Key Features

- Compliant with ATSC digital television standard
- Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
- Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
- Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
- NTSC interference rejection capability
- Compensate echo up to -5 to +47us range for terrestrial HDTV reception
- On-chip 10-bit ADC for HDTV/CATV demodulator
- On-chip programmable gain amplifier
- 25MHz crystal for clock generation
- On-chip PLL clock generation
- Full-digital timing recovery, no VCXO is required
- Full-digital frequency offset recovery with wide acquisition range ± 1 MHz for ATSC and ± 250 KHz for CATV reception
- Dual digital AGC controls for IF and RF respectively
- MPEG-2 transport stream output in parallel or serial format
- On-chip error rate estimators for TS packets, TCM decoder, and equalizer
- EIA/CEA-909 antenna interface
- Controlled by I²C interface
- Supports sleep mode to save power consumption
- Core power supply: 1.8V, peripheral power supply: 3.3V
- 100-LQFP package
- Lead Free

Functional Block Diagram

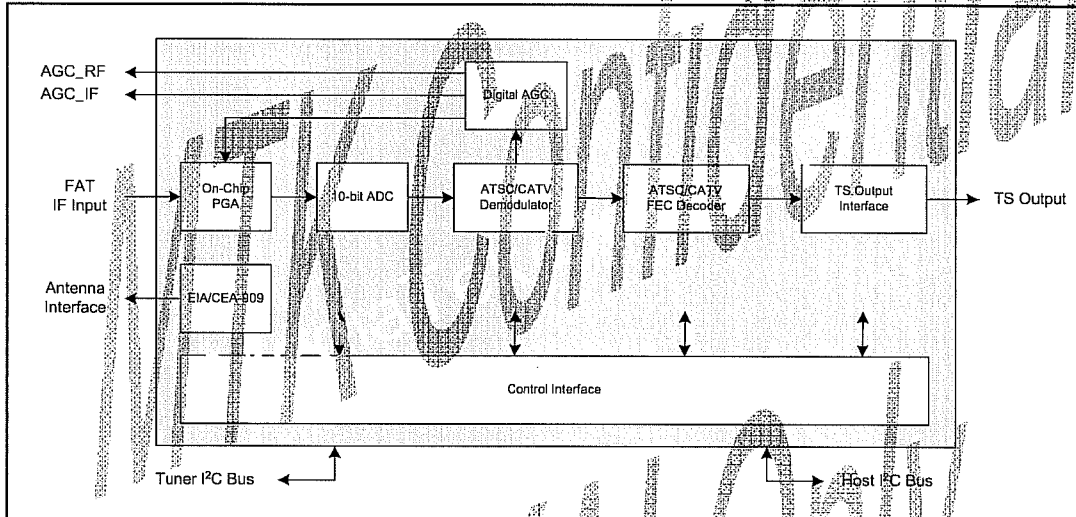


Figure 1: MT5111CE Functional Block Diagram

General Description

MT5111CE is a fully integrated single-chip 8-VSB and 64/256-QAM demodulator. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

MT5111CE includes a 10-bit A/D converter, 8-VSB/QAM demodulator, TCM (Trellis-Coded Modulation) decoder, and Reed-Solomon Forward Error Correction decoder. Moreover, an internal controller handles the acquisition and tracking to ensure the best receiving performance. The internal controller communicates with the external host controller via the I2C-compatible interface, and also provides direct control to the RF tuner via the second I2C-compatible

interface.

MT5111CE accepts either the direct IF signals centered at 44MHz or 43.75MHz, or the low IF signals centered at 5.38MHz. The center frequency of the incoming IF signal can also be programmed to other frequencies for various applications. An On-chip programmable gain-controlled amplifier is designed to provide sufficient signal amplitude when the received RF signal is weak. The IF signal is first sampled by a 10-bit A/D converter. Afterward, the digitized samples are further processed for adjacent channel interference rejection.

MT5111CE measures the power level of the digitized sequence, and feeds the control voltages back to the RF tuner and the IF amplifier respectively. The control voltages are converted to analog signals through the on-chip 1-bit sigma-delta D/A converters plus the off-chip R-C low-pass filters. The automatic gain control keeps the received power level at a desired level and maximizes the received SNR.

The carrier frequency offset and symbol timing offset are both estimated and compensated by a fully digital synchronizer. The synchronizer also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset. All synchronization in MT5111CE are integrated in digital circuits, no external VCXO is required.

The equalizer is adopted to cancel the effect of multi-path fading channel during signal propagation in the air or over cable networks. The equalizer is not only capable of acquiring correct coefficients combination by specified adaptive algorithms, but also programmable to different configurations for various channel conditions.

The following FEC decoder corrects most of the errors by the concatenation

of TCM and Reed-Solomon decoders. For CATV reception, MT5111CE detects and aligns de-puncturing timing of the received sequence. The timing synchronization is also automatically performed to lock the FEC frames. The on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: equalizer output, TCM decoder, and transport stream packets. The chip finally outputs the decoded MPEG-2 packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5111CE also provides the capability to remove the NTSC co-channel interference. To achieve the best reception condition, an antenna interface compliant with EIA/CEA-909 is designed to control the antenna parameters.

MT5111CE is designed with efficient mechanisms of power saving. When configured to enter the sleep mode by the system host, it can immediately turn off almost all embedded hardware except the on-chip controller to reduce the power consumption. Resuming from sleep mode is also triggered by the system host. Upon returning to the operation mode, the chip will try to re-acquire the DTV signal automatically.

Pin Out

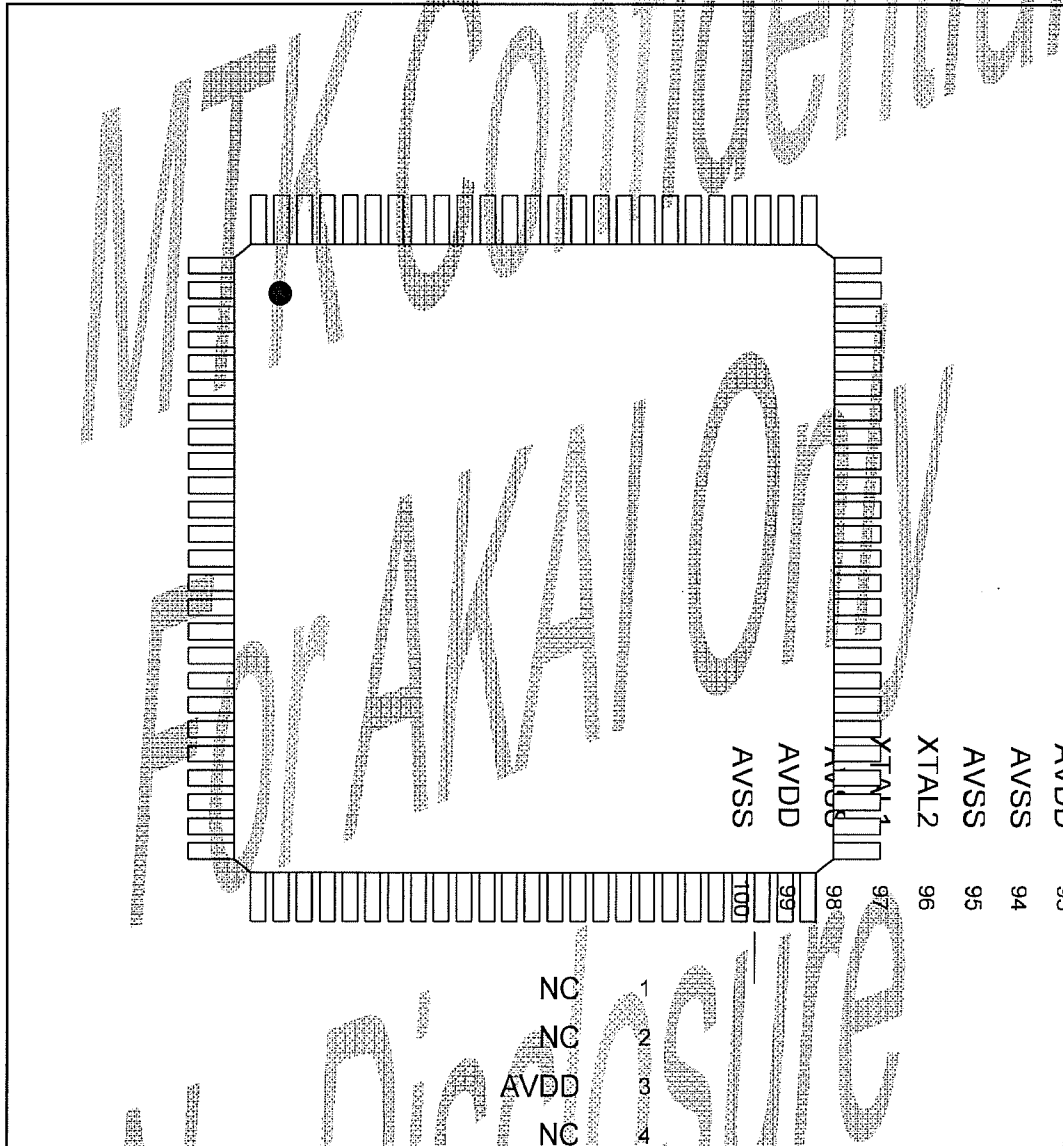


Figure 2: MT5111CE Pin Out

AVSS	7
NC	8
NC	9
AVDD	10
AVSS	11
AVDD	12
NC	13
NC	14
ADVDD3.3	15

Pin Description

Signal Name	Pin No	I/O	Description
Transport Stream			
TSDATA[7:0]	22,23,24,25,28, 29,32,33	O	TS data output
TSSYNC	34	O	TS packet start signal
TSVAL	38	O	TS output valid signal
TSCLK	37	O	TS output clock
TSERR	39	O	TS packet error indicator
Analog Signal			
IN+	82	I	Analog differential IF input
IN-	81	I	
REFTOP	88	O	ADC reference top voltage. Decouple with a capacitor to AVSS
REFBOT	86	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
VCMEXT	87	O	ADC common mode voltage
Antenna Interface			
ANTIF	62	O	CEA-909 Antenna Control Interface
Clock Generation			
XTAL1	97	I	25MHz crystal input
XTAL2	96	I	
Control Signals			
HOST_CLK	47	I	Host processor serial clock input, 5 volt compatible
HOST_DATA	44	I/O	Host processor serial data pin, 5 volt compatible
TUNER_CLK	69	O	Tuner serial clock output, 5 volt compatible
TUNER_DATA	68	I/O	Tuner serial data pin, 5 volt compatible
IF_AGC	72	O	IF AGC output
RF_AGC	73	O	RF AGC output
RESET	48	I	Power reset pin, low active
SA0	66	I	Chip slave address selection pin, tie to VDD3.3 or DGND
SA1	67	I	Chip slave address selection pin, tie to VDD3.3 or DGND
Power Supply			
VDD3.3	17,26,35,42, 52,60,70	P	Digital power supply, tie to 3.3V
VDD1.8	18,30,40,45, 55,64,75	P	Digital power supply, tie to 1.8V
DGND	16,19,27,31, 36,41,43,46,51,56, 61,63,65,71,74	P	Digital ground, tie to digital ground plane
AVDD	3,10,12,80,83,91, 92,93,99	P	Analog power supply, tie to 3.3V
AVSS	7,11,79,85,89,94, 95,98,100	P	Analog ground, tie to analog ground plane
ADVDD3.3	15,76	P	Digital power supply for analog component, tie to 3.3V
AVDD1.8	90	P	Digital power supply for analog component, tie to 1.8V
Others			
NC	1,2,4,5,6,8,9,13,14, 20,21,49,50,53,54, 57,58,59,77,78,84		Not Connected

Table 1: Pin Description

Electrical Characteristic

Recommended Operating Condition

Symbol	Description	Min	Typical	Max	Unit
T _j	Chip Junction Temperature	-	-	125	°C
VDD1.8	1.8V Digital Core Power Supply Voltage	1.62	1.8	1.98	Volt
AVDD	3.3V Analog Power Supply Voltage	3.15	3.3	3.45	Volt
VDD3.3	3.3V Digital IO Power Supply Voltage	3	3.3	3.6	Volt
AVDD1.8	1.8V Analog Power Supply Voltage	1.7	1.8	1.9	Volt
V _{IH}	Digital Input High Voltage	3	3.3	3.6	Volt
V _{IL}	Digital Input Low Voltage	-	0		Volt

Table 2: Recommend Operating Condition

Typical Current and Power Dissipation (ASTC Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	350	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	16	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	630	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital IO Power Dissipation	52.8	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	917.4	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 3: Typical Current and Power Dissipation (ATSC Mode)

Typical Current and Power Dissipation (QAM Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	175	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	19	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	315	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital I/O Power Dissipation	62.7	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	612.3	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 4: Typical Current and Power Dissipation (QAM Mode)



Specifications are subject to change without notice.

HDMI PanelLink Cinema Receiver

MT8293 is a low-cost, fully HDMI-compliant receiver that fits directly into home theater products such as LCD TVs, plasma TVs and HDTVs. The receiver is capable of supporting bandwidths up to 165MHz and video resolutions up to 1080p and UXGA. The MT8293 supports the DVD-Audio standard, including 7.1- surround audio at 96kHz and stereo audio at 192kHz.

The built-in High-bandwidth Digital Content Protection (HDCP) decryption engine secures the digital link for transmission of valuable high-definition video and audio. Built-in HDCP self-test engine simplifies manufacturing testing.

FEATHRES

■ Industry-Standard

- HDMI 1.1
- DVI 1.0
- EIA/CEA-861B
- HDCP 1.1

■ Digital Video Output

- Integrated PanelLink Core
- Supports DTV (480i/576i/480p/576p/720p/1080i/1080p) and PC (VGA/XGA/SXGA/UXGA) resolution up to 165MHz (using dual edge to transmit video data for pixel clock over 112MHz)
- Flexible digital video interface
 - 24-bit RGB/YCbCr 4:4:4
 - 16-bit YCbCr 4:2:2
 - 8-bit YcbCr 4:2:2 (ITU-R BT.656)
- Integrated RGB <-> YCbCr color space conversion (both 601 and 709)
- 4:2:2 <-> 4:4:4 converter
- Integrated Deinterlacer for 480i/576i (SDTV only)
- Integrated Down-Scaler (with CEN)

■ Digital Audio Output

- Industry-standard S/PDIF and 3-wire output

- Supports high-end audio including DVD-Audio
 - 2-ch. 32-192kHz or
 - 8-ch. 32-96kHz
- Programmable 3-wire output supports numerous low-cost I2S audio DACs
- Supports IEC60958 2-channel PCM
- Capable of carrying IEC61937 compressed audio (Dolby Digital, DTS, etc.)

■ Content Protection

- Integrated HDCP cipher engine
- External EEPROM for encrypt HDCP keys
- Built-in HDCP self-test
- Decrypts both video and audio

■ System Operation

- Register-programmable via slave I2C interface
- Auto video mode
- Auto audio mode
- Flexible interrupt registers with interrupt pin

■ Power Management

- 1.8V core provides low-power operation
- Flexible power-down modes

■ Outline

- 128-pin QFP package



MT8293

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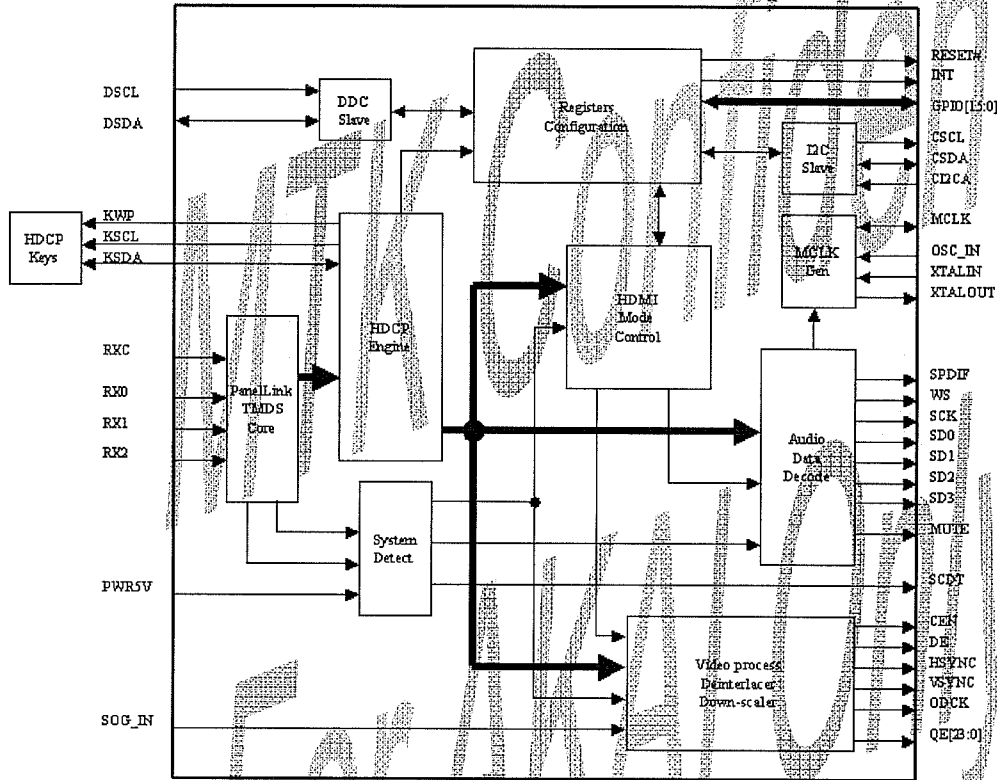
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CGND18	85	32	GP103
CVCC18	86	31	IOVCC33
MUTE	87	30	IOGND33
IOVCC33	88	29	GP104
IOGND33	89	28	GP105
SPDIF	70	27	GP106
SD3	71	26	GP107
SD2	72	25	CGND18
SD1	73	24	CVCC18
SD0	74	23	GP108
WS	75	22	GP109
SCK	76	21	GP110
IOVCC33	77	20	GP111
IOGND33	78	19	IOVCC33
MCLK	79	18	IOGND33
CGND18	80	17	GP112
CVCC18	81	16	GP113
AUXP_VCC18	82	15	GP114
AUXPGND	83	14	GP115
XTALOUT	84	13	CGND18
XTALIN	85	12	CVCC18
XTALVCC	86	11	K3CL
REGVCC	87	10	K3DA
RSVDL	88	9	K3MP
RESET#	89	8	NC
SCDT	90	7	IOVCC33
INT	91	6	IOGND33
QE23	92	5	NC
QE22	93	4	OSC_IN
QE21	94	3	SOG_IN
QE20	95	2	CEN
QE19	96	1	VSYN
		126	HSYN
		127	DE
		128	CGND18
		125	CVCC18
		124	DE
		123	DE
		122	DE
		121	DE
		120	IOVCC33
		119	IOVCC33
		118	IOGND33
		117	DE
		116	DE
		115	DE
		114	DE
		113	CGND18
		112	CVCC18
		111	DE
		110	DE
		109	DE
		108	DE
		107	IOVCC33
		106	IOGND33
		105	DE
		104	DE
		103	DE
		102	DE
		101	DE
		100	DE
		99	DE
		98	IOVCC33
		97	IOGND33



MT8293

No Disclosure



FOR ANALYSIS ONLY

NO DISCLOSURE

Item	Symbol	Pin #	Type	Description
DIGITAL				
Power/Ground (45)				
1	CVCC18	12,24,36,45,66,81,112,125	I	Digital Logic 1.8V power
2	CGND18	13,25,37,65,80,113,126	I	Digital Logic ground
3	IOVCC33	7,19,31,68,77,98,107,120	I	Input/Output Pin 3.3V power
4	IOGND33	6,18,30,69,78,97,106,118	I	Input/Output Pin ground
5	AVCC	49,53,57,61	I	TMDS Analog 3.3V power
6	AGND	52,56,60,64	I	TMDS Analog ground
7	PVCC	47	I	TMDS PLL 3.3V power
8	PGND	46	I	TMDS PLL ground
9	AUDPVCC18	82	I	ACR PLL 1.8V power
10	AUDPGND	83	I	ACR PLL ground
11	XTALVCC	86	I	ACR PLL crystal input 3.3V power
12	REGVCC	87	I	ACR PLL regulator 3.3V power
Configuration/Programming (20)				
1	INT	91	O	Interrupt output
2	RESET#	89	I	Reset Pin. Active low
3	DSCL	42	I	DDC I2C clock, 5V tolerance
4	DSDA	41	I/O	DDC I2C data, 5V tolerance
5	CSCL	40	I	Configuration I2C clock
6	CSDA	39	I/O	Configuration I2C data
7	KSCL	11	O	KEYS EEPROM I2C clock
8	KSDA	10	I/O	KEYS EEPROM I2C data
9	KWP	9	O	KEYS EEPROM write protect
10	SCDT	90	O	Indicates active video at HDMI input port
11	CISCA	38	I	I2C device address select



Item	Symbol	Pin #	Type	Description
12	PWR5V	44	I	TMDS port transmitter detect (hot plug), 5V tolerance
13	RSVDL	88	I	Must be tied low
14	RSVD	48	O	
15	NC	43	-	No connect
16	NC	8,5	-	No connect
17	OSC_IN	4	I	Oscillator input, External in
18	SOG_IN	3	I	SOG input, External AD in
19	CEN	2	O	Clock enable, for 8202 CEN input
Digital Audio Interface (9)				
1	MCLK	79	I/O	Audio master clock input reference
2	SCK	76	O	I2S serial clock output
3	WS	75	O	I2S word select output
4	SD0	74	O	I2S serial data output
5	SD1	73	O	I2S serial data output
6	SD2	72	O	I2S serial data output
7	SD3	71	O	I2S serial data output
8	SPDIF	70	O	S/PDIF audio output
9	MUTE	67	O	Mute audio output
GPIO Interface (16)				
1	GPIO0	35	I/O	GPIO
2	GPIO1	34	I/O	GPIO
3	GPIO2	33	I/O	GPIO



Item	Symbol	Pin #	Type	Description
4	GPI03	32	I/O	GPIO
5	GPI04	29	I/O	GPIO
6	GPI05	28	I/O	GPIO
7	GPI06	27	I/O	GPIO
8	GPI07	26	I/O	GPIO
9	GPI08	23	I/O	GPIO
10	GPI09	22	I/O	GPIO
11	GPI010	21	I/O	GPIO
12	GPI011	20	I/O	GPIO
13	GPI012	17	I/O	GPIO
14	GPI013	16	I/O	GPIO
15	GPI014	15	I/O	GPIO
16	GPI015	14	I/O	GPIO
TTL Interface (28)				
1	DE	127	O	Data enable
2	VSYNC	1	O	Vertical sync
3	HSYNC	128	O	Horizontal sync
4	ODCK	119	O	Output data clock
5	QE0	124	O	24-bit Even pixel
6	QE1	123	O	24-bit Even pixel
7	QE2	122	O	24-bit Even pixel

Item	Symbol	Pin #	Type	Description
8	QE3	121	O	24-bit Even pixel
9	QE4	117	O	24-bit Even pixel
10	QE5	116	O	24-bit Even pixel
11	QE6	115	O	24-bit Even pixel
12	QE7	114	O	24-bit Even pixel
13	QE8	111	O	24-bit Even pixel
14	QE9	110	O	24-bit Even pixel
15	QE10	109	O	24-bit Even pixel
16	QE11	108	O	24-bit Even pixel
17	QE12	105	O	24-bit Even pixel
18	QE13	104	O	24-bit Even pixel
19	QE14	103	O	24-bit Even pixel
20	QE15	102	O	24-bit Even pixel
21	QE16	101	O	24-bit Even pixel
22	QE17	100	O	24-bit Even pixel
23	QE18	99	O	24-bit Even pixel
24	QE19	96	O	24-bit Even pixel
25	QE20	95	O	24-bit Even pixel
26	QE21	9	O	24-bit Even pixel
27	QE22	93	O	24-bit Even pixel
28	QE23	92	O	24-bit Even pixel



Item	Symbol	Pin #	Type	Description
ANALOG (8)				
Differential signal				
1	RXC+	51	I	TMDS input clock pair
1	RXC-	50	I	TMDS input clock pair
1	RX0	55	I	TMDS input data pair
1	RX0	54	I	TMDS input data pair
1	RX1	59	I	TMDS input data pair
1	RX1	58	I	TMDS input data pair
1	RX2	63	I	TMDS input data pair
1	RX2	62	I	TMDS input data pair
PLL group(2)				
68	XTALIN	85	I	Crystal input PAD
69	XTALOUT	84	O	Crystal output PAD

No Disclosure



MTK

MT8202

Specifications are subject to change without notice.

HDTV-Ready LCD TV Chip

MT8202 is a highly integrated single chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals. Embedded HDTV/VGA decoders let the high bandwidth input signals perfectly reproduced. 24/16/8 bits digital port may accept all kinds of external digital input video source. New 2nd generation advanced motion adaptive de-interlacer converts accordingly the interlace video into progressive one with overlay of a 2D Graphic processor. Advanced full function color processing with fully 10-bit path provides high quality video contents. Independent two Flexible scalers provide wide adoption to various LCD panels for two of different video sources at the same time. Its on-chip audio processor decodes analog signals from tuner with lip sync control, delivering high quality post-processed sound effect to customers. On-chip microprocessor reduces the system BOM and shortens the schedule of UI design by high level C program. MT8202 is a cost-effective and high performance HDTV-ready solution to LCD TV manufactures.

FEATURES

■ Video Input

- Support fully programmable 8 Composite/SV input pins
- Support 2 Component inputs with SDTV format & HDTV 480p/720p/1080i format
- Support 1 VGA input up to SXGA (1280x1024x75Hz) including SOG signals
- Support DVI 24-bit RGB digital input
- Support CCIR-656/601 digital input

■ TV decoder

- Full 10-bit data path to enhance the video resolution and reduce digital truncation errors
- Support PAL (B, G, D, H, M, N, I, Nc), PAL (Nc), PAL, NTSC, NTSC-4.43, SECAM
- Automatic Luma/Chroma gain control

- Automatic TV standard detection
- 2nd generation NTSC/PAL Motion Adaptive 3D comb filter with huge improvement
- Motion Adaptive 3D Noise Reduction
- VBI decoder for Closed-Caption/XDS/Teletext/WSS/VPS
- High speed advanced Teletext/Closed-Caption drawing engine directly on OSD plane
- Macrovision detection
- Adjustable horizontal delay for combination of SCART Composite/RGB input

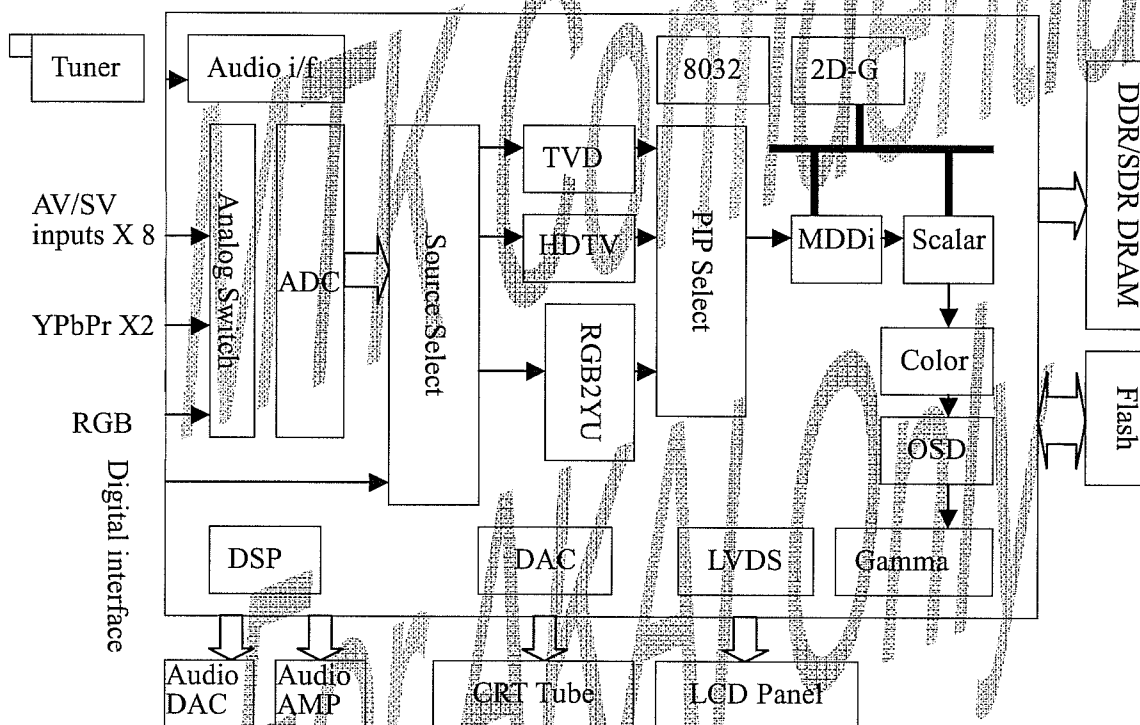
■ Video Processor

- Fully 10-bit processing to enhance the video quality
- Advanced flesh tone and color processing
- Gamma/anti-Gamma correction
- Advanced Color Transient Improvement (CTI)
- 2D Peaking
- Advanced horizontal/vertical sharpness
- Saturation/hue adjustment
- Brightness and contrast adjustment
- Black level extender
- White peak level limiter
- Adaptive Luma/Chroma management
- Automatic detect film or video source
- 3:2/2:2 pull down source detection
- 2nd generation Advanced Motion adaptive de-interlacing
- Arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X
- Advanced linear and non-linear Panorama scaling
- Programmable Zoom viewer
- Progressive scan output
- Picture-in-Picture (PIP)
- Picture-Out-Picture (POP)
- Advanced dithering processing for LCD display with 6/8/10 bit output
- Frame rate conversion, 50Hz to 75Hz

■ Audio DSP

- Support BTSC/EIAJ/A2/NICAM decode
- Stereo demodulation, SAP demodulation

- Noise reduction
- Mode selection (Main/SAP/Stereo)
- Pink noise and white noise generator
- Equalizer
- Sub-woofer/Bass enhancement
- Noise auto mute
- 3D surround processing include virtual surround
- Audio and video lip synchronization
- Support Reverberation
- Audio Input/Output
 - Decode audio AF from Tuner
 - 2 channel audio L/R digital line in
 - 7.1-channel slave digital line in
 - Including full 7.1-channels digital output, 2-channel bypass and 2-channel headphone output
 - Embedded 3 internal DAC output
- DRAM Controller
 - Supports up to 32M-byte SDR/DDR DRAM
 - Supports 2x16 bit SDR/DDR bus interfaces
 - Build in a DRAM interface programmable clock to optimize the DRAM performance
 - Programmable DRAM access cycle and refresh cycle timings
 - Support 3.3/2.5-Volt SDR/DDR interface
- Video Output
 - TV pattern generator for testing
 - Interlaced 50Hz to 120Hz
 - Support up to 1366 horizontal points
 - 6/8/10-bit single channel or 6/8/10-bit dual channel LVDS output
 - Support video output mirror and upside down
- 2D-Graphic/3 OSD processor
 - Embedded Two backend RGB domain OSD planes and one YUV domain OSD
 - Support Text/Bitmap decoder
 - Support line/rectangle/gradient fill
 - Support bitblt
 - Support color Key function
 - Support Clip Mask
 - Support Alpha blending with video output
 - 65535/256/16/4/2-color bitmap format OSD,
 - Automatic vertical scrolling of OSD image
 - Support OSD mirror and upside down
- Host Micro controller
 - Turbo 8032 micro controller
 - Built-in internal 373 and 8-bit programmable lower address port
 - 2048-bytes on-chip RAM
 - Up to 4M bytes FLASH-programming interface
 - Supports 5/3.3-Volt FLASH interface
 - Supports power-down mode
 - Supports additional serial port
 - IR control serial input
 - Support 2 RS232 interface for external source communication
 - Support 2 PWM output
 - Support DDC2Bi/DDC2B/DDC1/DDCCI
 - Programmable GPIO setting for complex external device control
- Outline
 - 388-pin BGA package
 - Lead Free
 - 3.3/2.5/1.8-Volt operating voltages
 - 0.18um process

BLOCK DIGRAM

Analog Switch

Analog switches are built in MT8202 to connect to 17 input signals and there is need to add external components to add analog video multiplexes on board.

There are 9 high-speed differential input pairs for 3 sets of YPRPB/VGA input signals.

The 8 Composite/S signal input pins can be fully programmed to connect to any AV/SV inputs.

ADC/ Source Select

The video ADC sample analog input signals. After ADC, all signal processing is digital domain. The source select multiplex all inputs from digital and analog video ports and route them into data path.

Audio Interface

Audio interface accept analog audio signal from Tuner, e.g. AF. It also includes preprocessing circuit to filter the noisy audio signals. Audio decoder will decode the BTSC or NICAM, and output best sound with enhanced 3D surround post-processing.

Embedded 7.1 channel digital audio input (slave) and 2 channels (master) digital audio inputs.

Embedded 3 high performance audio DACs.

DSP



DSP handle audio decoding as well as computing intensive jobs. The downloadable micro code enables fast function convergence for various audio standards in the world.

Advanced DSP engine supports full functions of sound effects.

MDDi/Scaler

MDDi is MTK proprietary de-interlacing technology. 2nd generation MDDi solution provides improved low angle processing and more accurate motion detection for all interlace sources. The techniques reduce jagged edges and broken images. The MDDi engine supports both Main and Sub channel SDTV inputs or one channel 1080i high quality de-interlacing.

Two totally independent scaler support full functions of PIP/POP and frame rate conversion.

With MDDi and high quality scaler, MT8202 guarantee all input format could be translated to output format with best video quality for motion and still pictures.

Color/Gamma

MT8202 includes advanced color management function to allow user to improve video quality with fully flexibility. With contrast/hue/saturation/Gamma/anti-Gamma/flesh tone function, MT8202 deliver the best video quality with vivid color.

Advanced dither function support 6/8/10-bit video output for any kinds of display unit (LCD, PDP, CRT).

8032

On-chip Turbo8032 provide the most cost effective development environment for system house. Well-proven FW could speed up the system design significantly.

2D-G/OSD

On-chip graphic engine draw bitmap OSD and store them into DRAM. OSD read data from DRAM and display on screen. With 2D-G and OSD. The computing power requirement of μP will be minimized.

One YUV space OSD added to support Main/PIP Teletext/Close-caption functions.



MTK

MT5351

Specifications are subject to change without notice.

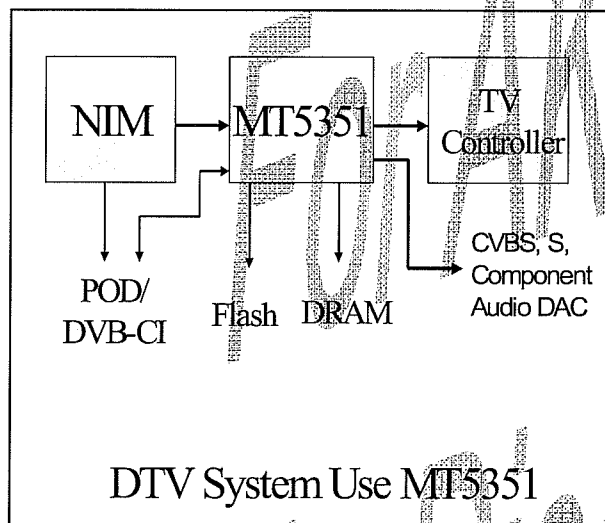
DTV Backend Decoder SOC

MediaTek MT5351 is a DTV Backend Decoder SOC which support flexible transport demux, HD MPEG-2 video decoder, JPEG decoder, MPEG1,2, MP3, AC3 audio decoder, HD TV encoder. The MT5351 enables consumer electronics manufacturers to build high quality, feature-rich DTV, STB or other home entertainment audio/video device.

World-Leading Technology: HW support worldwide major broadcast network and CA standards, include ATSC, DVB, OpenCable, DirectTV, MHP.

Rich Feature for high value product: To enrich the feature of DTV, the MT5351 support 1394-5C component to external DVHS. Dual display, PIP/POP and quad pictures provide user a whole new viewing experience.

Credible Audio/Video Quality: The MT5351 use advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. The embedded 4X over-sample video DAC could generate very fine display quality. Also, the audio 3D surround and equalizer provide professional entertainment



Key Features:

1. Flexible Demuxer
2. Dual HD MPEG2 Video Decoder
3. Dual MPEG1,2, MP3, AC3 Audio decode
4. Dual Display
5. PIP/POP/Quad Mode
6. IEEE1394-5C
7. POD/DVB-CI

Application:

1. DTV
2. Set-top Box
3. DTV Recorder
4. Home Media Center

Order Information:

MT5351AG → one HD decoder
 MT5351CG → two HD decoder
 All Package are Lead Free

M ARM
 MT5351AG
 DDDD-BC#L
 LLLLL

IC Top View:
 DDDD: Date Code
 #: Subcontractor Code
 LLLLL: Lot Number

General Feature List

- **Host CPU**
 - ARM 926EJ
 - 16K I-Cache and 16K D-Cache
 - 8K Data TCM and 8K Instruction TCM
 - JTAG ICE interface
 - Watch Dog timers
- **Transport Demuxer**
 - Support 3 independent transport stream inputs
 - Support serial / parallel interface for each transport stream input.
 - Support ATSC, DVB, and MPEG2 transport stream inputs
 - Programmable sync detection.
 - Support DES/3-DES de-scramble
 - 96 PID filter and 128 section filters.
 - Support TS recording via IEEE1394 interface
- **MPEG2 Decoder**
 - Support dual MPEG-2 HD decoder or up to 8 SD decoder
 - Complaint to MP@ML, MP@HL and MPEG-1 video standards
- **JPEG Decoder**
 - Decode Base-line or progressive JPEG file
- **2D Graphics**
 - Support multiple color modes
 - Point, horizontal/vertical line primitive drawing
 - Rectangle fill and gradient fill functions
 - Bitblt with transparent, alpha blending, alpha composition and stretch
 - Font rendering by color expansion
 - Support clip masks
 - YCbCr to RGB color space transfer
- **OSD Display**
 - 3 linking list OSDs with multiple color mode
 - OSD scaling with arbitrary ratio from 1/2x to 2x
 - Square size, 32x32 or 64x64 pixel, hardware cursor
- **Video Processing**
 - Advanced Motion adaptive de-interlace on SDTV resolution
 - Support clip
 - 3:2:2 pull down source detection
 - Arbitrary ratio vertical/horizontal scaling of video, from 1/15X to 16X
 - Support Edge preserve
 - Support horizontal edge enhancement
 - Support Quad-Picture
- **Main Display**
 - Mixing two video and three OSD and hardware cursor
 - Contrast/Brightness adjustment
 - Gamma correction
 - Picture-in-Picture (PIP)
 - Picture-Out Picture (POP)
 - 480i/576i/480p/576p/720p/1080i output
- **Auxiliary Display**
 - Mixing one video and one OSD
 - 480i/576i output
- **TV Encoder**
 - Support NTSC M/N, PAL M/N/B/D/G/H/I
 - Macrovision Rev 7.1.L1
 - CGMS/WSS
 - Closed Captioning
 - Six 12-bit video DACs for CVBS, S-video or RGB/YPbPr output
- **Digital Video Interface**
 - Support SA/EAV
 - Support 8/16 for SD/HD digital video input
 - Support 8/16/24 bits digital output for main display
 - Support 8 bits digital output for aux display
- **DRAM Controller**
 - Supports 64Mb to 1Gb DDR DRAM devices
 - Configurable 32/64 bit data bus interface
 - Support DDR266, DDR333, DDR400 JEDEC specification compliant SDRAM
- **Peripheral Bus Interface**
 - Support NOR/NAND flash
 - Support CableCard host control bus
- **Audio**

- Support Dolby Digital AC-3 decoding
 - MPEG-1 layer I/II, MP3 decoding
 - Dolby prologic II
 - Main audio output: 5.1ch + 2ch (down mix)
 - Auxiliary audio output: 2ch
 - Pink noise and white noise generator
 - Equalizer
 - Bass management
 - 3D surround processing include virtual surround
 - Audio and video lip synchronization
 - Support reverberation
 - SPDIF out
 - I2S I/F
- Peripherals
- Three UARTs with Tx and Rx FIFO, two of them have hardware flow control
 - Two serial interfaces, one is master only, the other can be set to master mode or slave mode
 - Two PWMs
 - IR blaster and receiver
 - IEEE 1394 link controller
 - IDE bus: ATA/ATAPI7 UDMA mode 5, 100 MB/s
 - Real-time clock and watchdog controller
 - Memory card I/F: MS/MS-Pro, SD, CF, and MMC
 - PCMCIA/POD/CI interface
- IC Outline
- 471 Pin BGA Package
 - 3.3V/1.2V dual Voltage

Electrical Characteristics

Absolute Maximum Rating

Symbol	Parameters	Value	Unit
IOVDD	3.3V supply voltage	-0.5 to 4.6	V
CVDD	1.2V supply voltage	-0.5 to 1.8	V
AVDD	Analog supply voltage	-0.5 to 4.6	V
RVDD	DDR supply voltage	-0.5 to 3.5	V
VIN(3.3V)	Input Voltage(3.3V IO)	VSS-1.0 to 3.63	V
VIN(5V tolerance)	Input Voltage(5V tolerance IO)	VSS-1.0 to 5.5	V
Vout	Output Voltage	-0.3 to VDD3+0.3	V
Ts	Storage Temperature	-40 to 150	C
Ta	Ambient Temperature	0 to 70	C

DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
IOVDD	3.3V supply voltage	2.97	3.3	3.63	V
CVDD	1.2V supply voltage	1.08	1.2	1.32	V
AVDD	Analog supply voltage	2.97	3.3	3.63	V
VIH(3.3V)	3.3V input voltage high	2.0			V
VIL(3.3V)	3.3V input voltage low			0.8	V
VOH(3.3V)	3.3V output voltage high	2.4			
VOL(3.3V)	3.3V output voltage low			0.4	
VIH(3/5V)	3/5V tolerance input voltage high	2.0			V
VIL(3/5V)	3/5V tolerance input voltage low			0.8	V
VOH(3/5V)	3/5V tolerance output voltage high	2.4			V
VOL(3/5V)	3/5V tolerance output voltage low			0.4	V
Tj	Junction operation temperature	-40	25	125	C
PD(estimate)	Power dissipation		1.5		W
Pdown	Power down mode		2		mW



DDR ELECTRICAL Characteristics and DC Operating Condition

Symbol	Parameters	Min	Typ	Max	Unit
RVDD(DDR333)	DDR I/O supply voltage for DDR266 or DDR333	2.3	2.5	2.7	V
RVDD(DDR400)	DDR I/O supply voltage for DDR400	2.5	2.6	2.7	V
DVREF	DDR I/O reference voltage	0.49*RVDD	0.5*RVDD	0.51*RVDD	V
VTT	DDR I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V
VIH	DDR input voltage high	VREF+0.15		RVDD+0.3	V
VIL	DDR input voltage low	-0.3		VREF-0.15	V

DDR AC Operating Condition

Symbol	Parameters	Min	Typ	Max	Unit
VIH	Input high voltage, DQ, DQS	DVREF+0.31			V
VIL	Input low voltage, DQ, DQS			DVREF-0.31	V
Vslew	Input minimum slew rate	1.0			V/ns
Vswing	Input maximum swing			1.5	V

Digital Power Amplifier R2S15102NP

10Wx2ch(SE)/20Wx1ch(BTL) Digital Audio Power Amplifier

1. Outline

R2S15102NP is a Digital Power Amplifier IC developed for TV.
R2S15102NP can realize maximum Power 10W × 2ch
(VD = 24V, THD = 10%, SE) at 8 Ω load.
It is possible to replace from the conventional analog amplifier
system to the digital amplifier system easily.

2. Feature

High Output Power(THD=10%)without external Heat Sink
(note) the thermal pad is soldered the thermal pad with
the printed-circuit board directly.

Recommended Power Condition

SE operation mode :10Wx2ch(VD=24V) at 8 Ω

BTL operation mode: 20Wx1ch(VD=18V) at 8 Ω

The RENESAS original circuits realize high power efficiency,
low noise and low distortion characteristics.

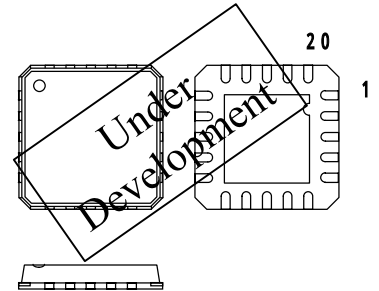
Pop sound Less

Built-in protection function

(Over Current, Over Temperature and Under Voltage)

Built-in Mute and Stand-by function

Fig. 1 Package



20pin QFN

Body : 6 x 6 mm

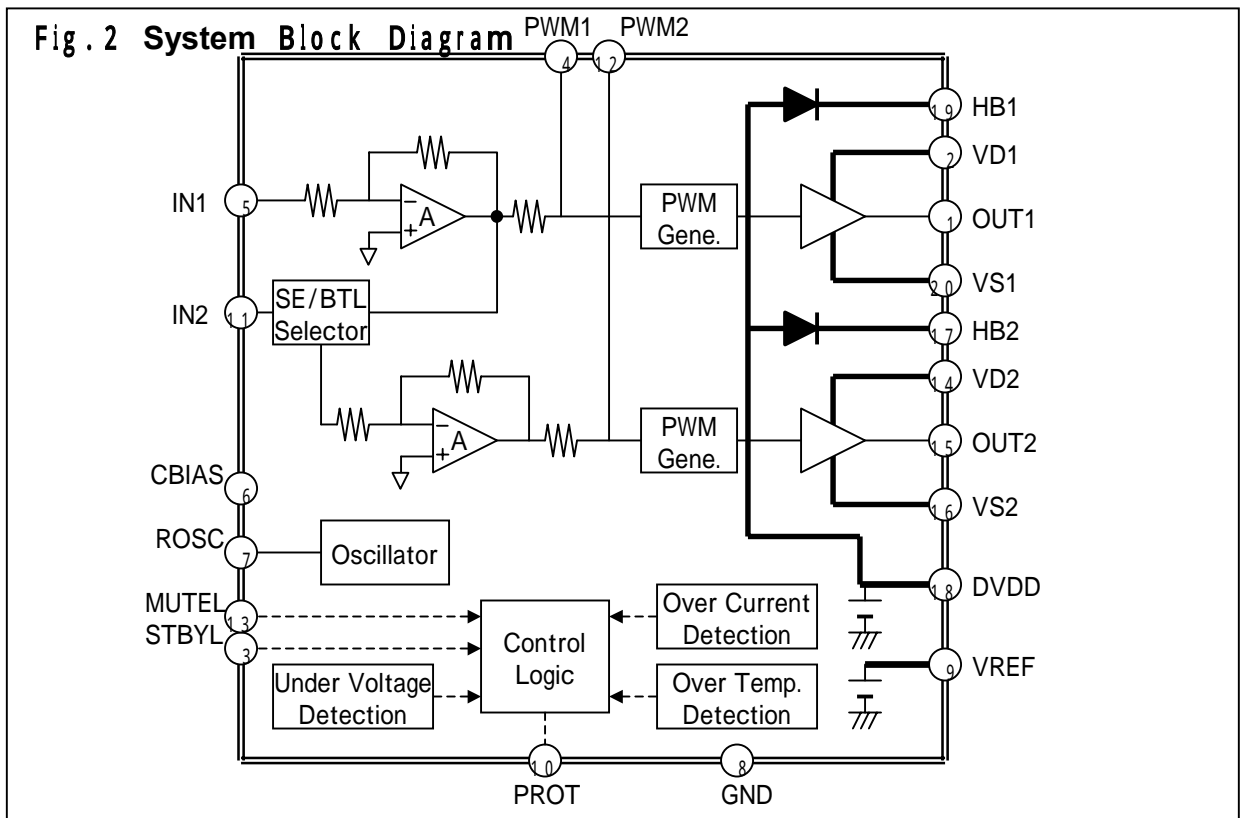
Lead pitch : 0.8 mm

3. Operating Condition

Recommended Power supply voltage : from 11V to 25V

Recommended Speaker Impedance : from 4 to 8Ω

4. Block Diagram



Digital Power Amplifier R2S15102NP

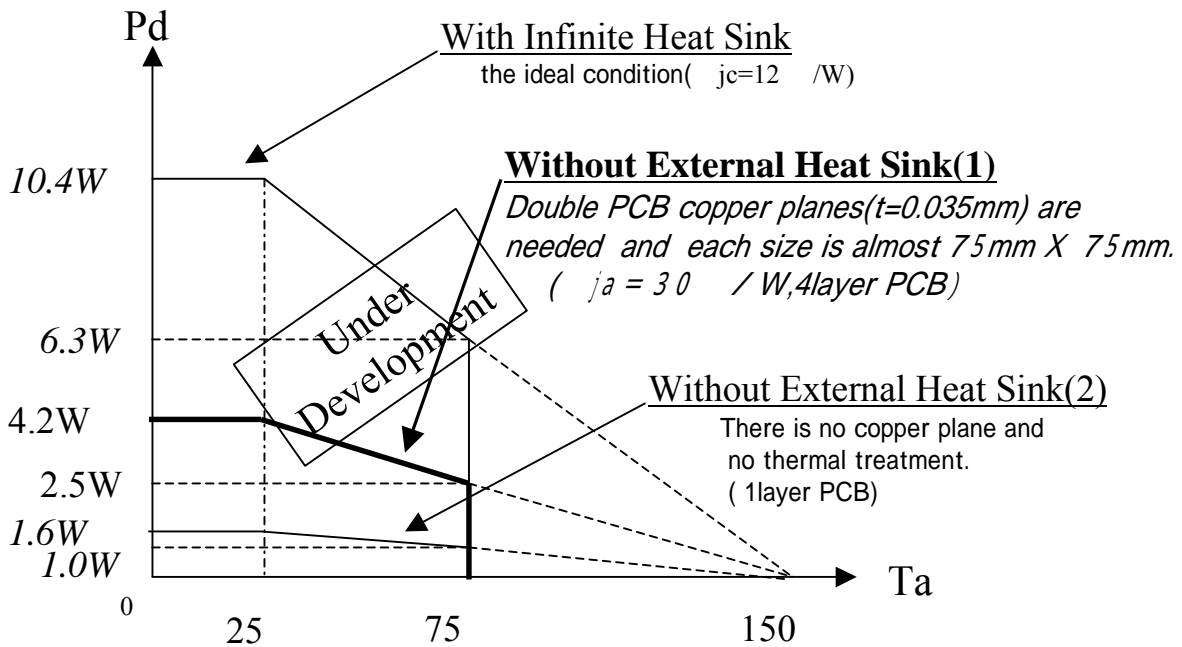
5 . Pin Configuration(Table.1)

No.	NAME	I/O	Description	
1	OUT1	O	Power Output pin #1	
2	VD1	-	Power supply pin for power output stage #2	
3	STBYL	I	Stand-by control pin. When this is “L”, circuit current is reduced. There is the pull-down resistor: 50Kohm(typ.).	
4	PWM1	I	PWM input pin #1 (for phase compensation)	
5	IN1	I	Analog input #1. The gain is depended on the external resistance .	
6	CBIAS	I/O	A capacitor is connected so that it may not be influenced of power supply change(Ripple Filter).	
7	ROSC	I	Control pin for PWM carrier frequency	
8	GND	-	GND pin for analog block	
9	VREF	I/O	Capacitor connection pin for analog block reference voltage source	
10	PROT	O	Protection Timer pin. At protection mode, the output becomes “L”-level. (The timing capacitor is connected)	
11	IN2	I	SE operation	Analog input #2(as same as IN1)
		I	BTL operation	When this is connected to DVDD pin via the resistor, Reversed signal of OUT1 is output to OUT2.
12	PWM2	I	PWM input pin#2 (for phase compensation)	
13	MUTEL	I	Mute control pin. When this is “L”, it becomes mute status.	
14	VD2	-	Power supply pin for power output stage #2	
15	OUT2	O	Power Output pin #2	
16	VS2	-	Ground pin for power output stage #2	
17	HB2	I/O	Capacitor connection pin for bootstrap	
18	DVDD	O	Built-in power supply pin for internal digital block.	
19	HB1	I/O	Capacitor connection pin for bootstrap #1	
20	VS1	-	Ground pin for power output stage #1	

6 . Absolute Maximum Rating(Table.2)

Symbol	Parameter	Condition	Value	Unit
VD max	Maximum VD Voltage	VD1,VD2 pin voltage	27	V
HB max	Maximum HB Voltage	HB1, HB2 pin voltage	40	V
Pd	Power dispassion	Ta = 25°C :See Fig.3	4.2	W
ja	Thermal Resistance	See Fig.3	30	/W
Tj	Junction temperature	Maximum Temperature	150	
Ta	Operating ambient temperature	Temperature range	-20 ~ 75	
Tstg	Storage temperature	Temperature range	-40 ~ 150	

Fig.3 Thermal De-rating(on PCB: printed-circuit board):Size 75mm x 75mm

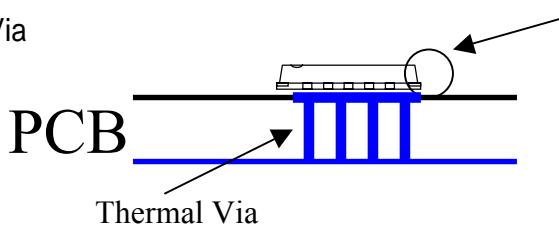


(NOTE)

PCB pattern design for high effective thermal conductivity

(1)The exposed die pad is **directly** soldered with the printed-circuit board pattern .

(2)Thermal Via



(caution)

There are side expositions of the die pad at corners of the package.

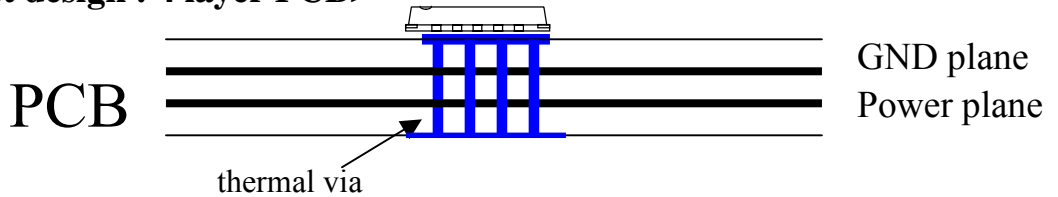
(The die pad is grounded.)

Consideration about the PCB design

The Power dissipation at 10Wx2ch(SE) or 20Wx1ch(BTL) is estimated almost 2W. It has enough margin, designing the PCB at $j_a=30$ /W.

(1)PCB basic design (copper plane)

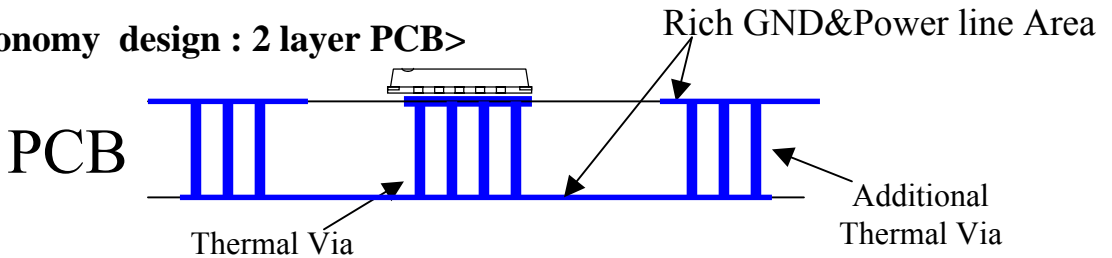
<the best design : 4 layer PCB>



<PCB size estimation >

10Wx2ch: 75mm x 75mm

<the economy design : 2 layer PCB>



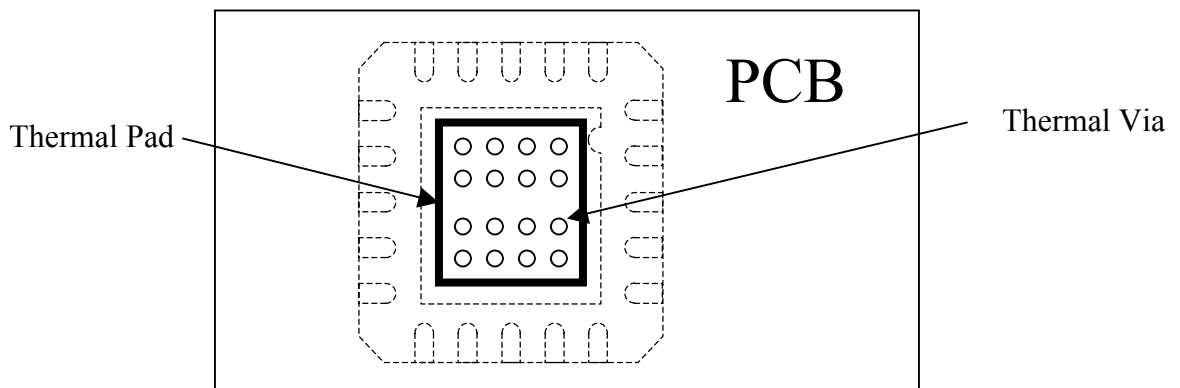
The GND&Power line total area size is also equal to the above GND&Power line total area size of the 4layer PCB.

<PCB size estimation >

10Wx2ch: (75+)mm x (75+) mm

(2)PCB Thermal Pad

The exposed die pad is **directly** soldered with the printed-circuit board pattern .



Digital Power Amplifier R2S15102NP

7 . Recommended Operating condition(Table.3)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VD	Supply Voltage	VD1,VD2 pin voltage	11	-	25	V
VH	Control voltage of high level	STBYL, MUTEL	2	-	5	V
VL	Control voltage of low level	STBYL, MUTEL	0	-	0.8	V
fosc	Carrier Frequency	R= 33k	300	400	600	kHz

- (note)
- STBYL: High level:normal operation Low level:Stand-by
 - MUTEL:High level:normal operation Low level:Mute
 - The carrier frequency can be changed by the resistance at Pin#.7 .

8 . Electronic Characteristics(Table.4)

(Unless otherwise noted, Ta=25°C, VD=24V, Carrier Frequency=400kHz, f=1kHz,SE operation)

Symbol	Parameter		Condition	MIN	TYP	MAX	Unit
IVD	Circuit Current		No Signal	TBD	28	TBD	mA
			MUTE	TBD	-	TBD	mA
			Stand-by	-	-	10	uA
VDPR	Detection Voltage		VD under-voltage	TBD	9.8	TBD	V
TPR	Protection Temperature		Thermal Shut-dawn	-	150	-	
TRL	Release Temperature		Thermal Shut-dawn	-	120	-	
IPR	Protection Current		Output over-current	-	6	-	A
Pomax	Maximum output power	at SE	THD=10%, VD=24V, RL=8	TBD	10	-	W/ch
		at BTL	THD=10%, VD=18V, RL=8	TBD	20	-	W
THD	Total Harmonic Distortion		Po=1W	-	0.1	TBD	%
No	Output Noise level		A-Weighted filter	-	(100)	TBD	uVrms
Eff	Power Efficiency	at SE	Po=10+10W	TBD	93	-	%
		at BTL	Po=20W	TBD	89	-	%
Mute	Mute Attenuation			TBD	80	-	dB
PSRR	Ripple Rejection Ratio		dVD=100mVrms,f=100 Hz	TBD	50	-	dB

9 . Application Examples

Fig.4 SE operation mode(10Wx2ch)

(note)

“R for GND” ‘s are for the evaluation only and not needed actually.

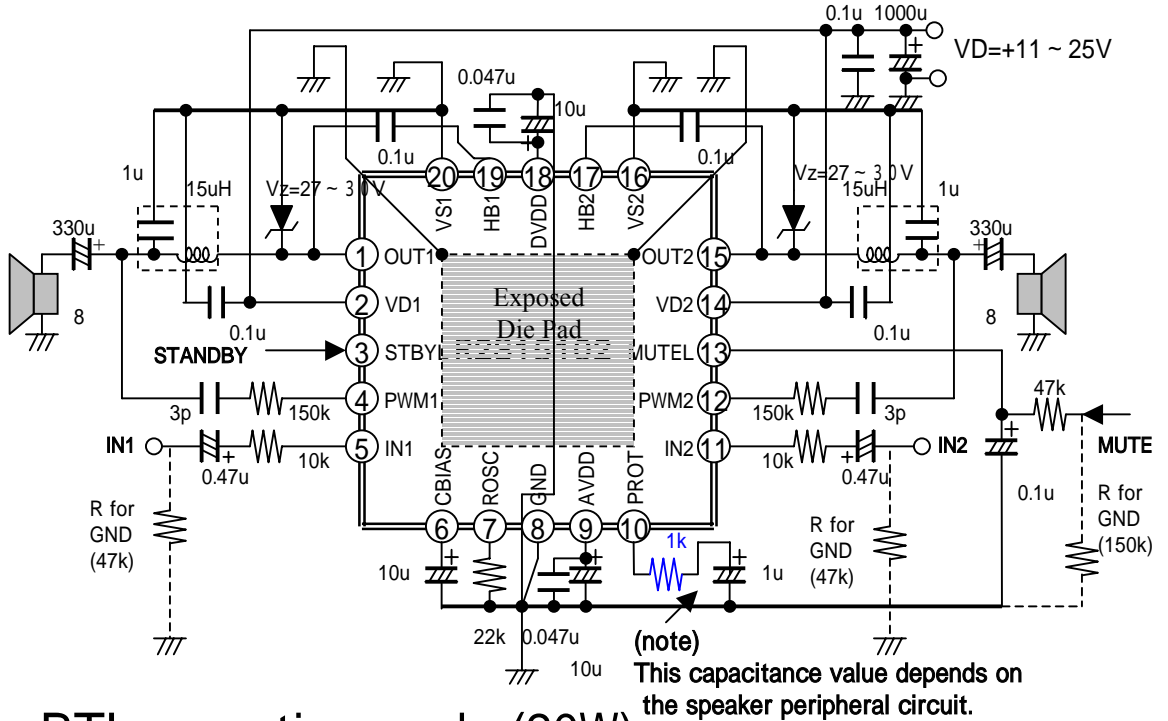
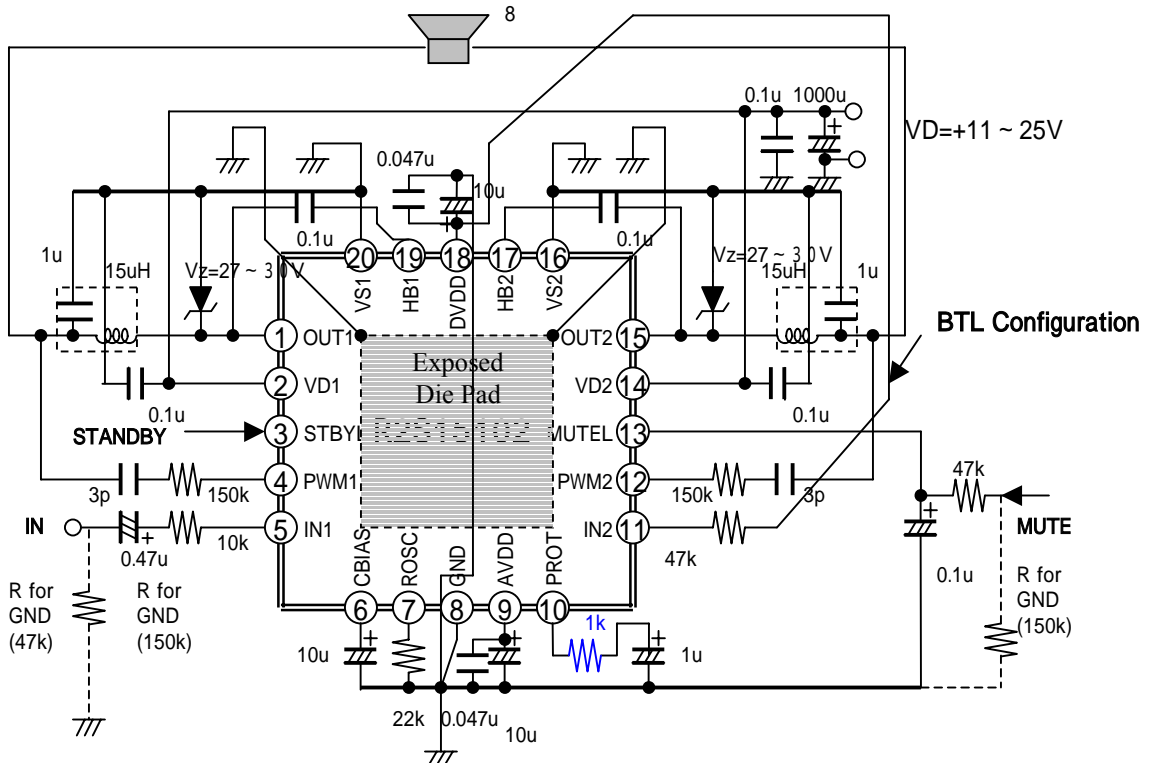


Fig.5 BTL operation mode (20W)



Digital Power Amplifier R2S15102NP

Fig.6 BTL operation mode(20W) with PWM direct input

(note)
“R for GND” ‘s are for the evaluation only and not needed actually.

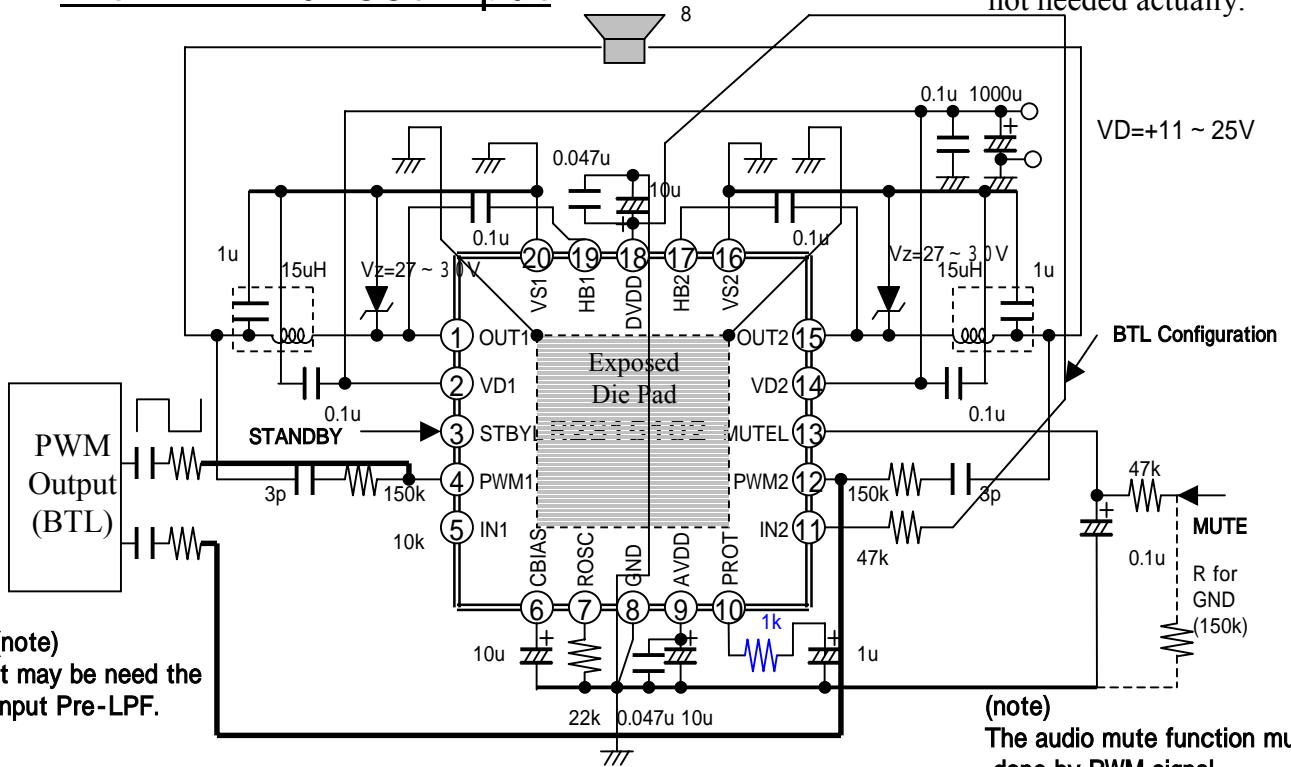
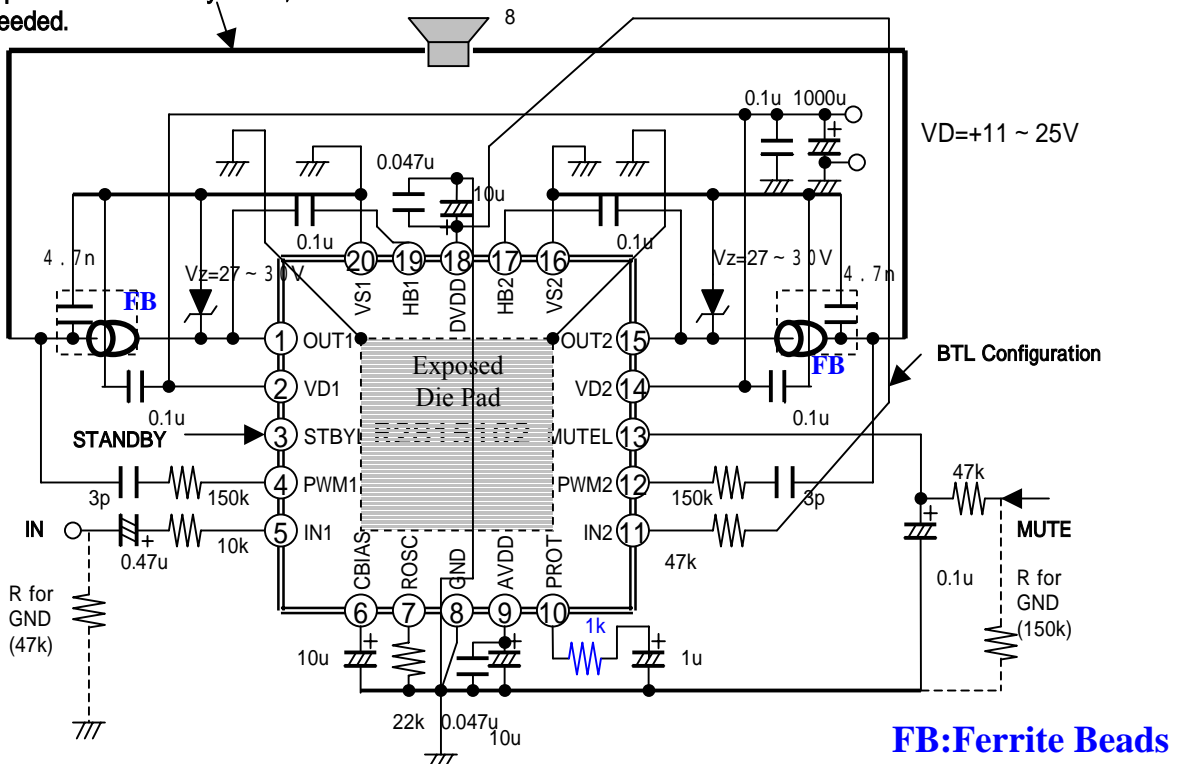


Fig.7 BTL operation mode without output LPF coil

If this speaker lines is very short, the LPF coil is not needed.



24-bit, 192kHz Stereo Codec with 5 Channel I/P Multiplexer

DESCRIPTION

The WM8776 is a high performance, stereo audio codec with five channel input selector. The WM8776 is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used with a five stereo channel input mixer. Each ADC channel has programmable gain control with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

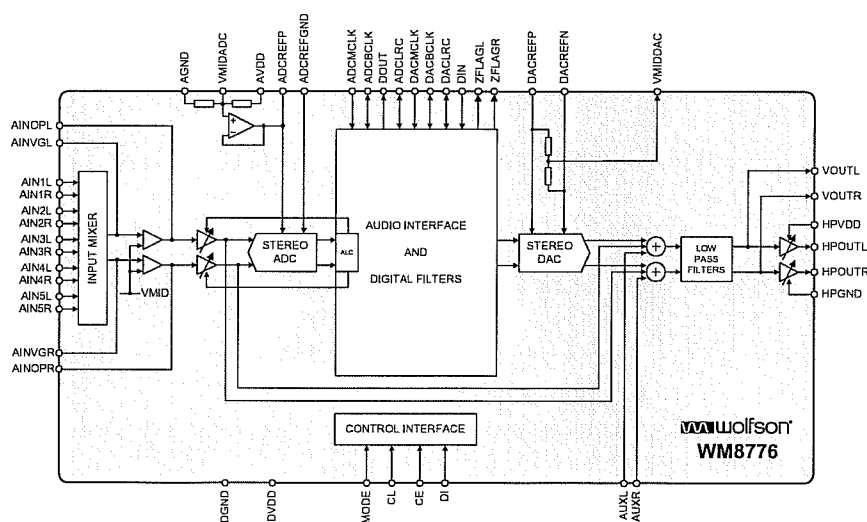
A stereo 24-bit multi-bit sigma delta DAC is used with digital audio input word lengths from 16-32 bits and sampling rates from 32kHz to 192kHz. The DAC has an input mixer allowing an external analogue signal to be mixed with the DAC signal. There are also Headphone and line outputs, with volume controls for the headphones.

The WM8776 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I²S, left justified, right justified and DSP formats.

The device is controlled in software via a 2 or 3 wire serial interface, selected by the MODE pin, which provides access to all features including channel selection, volume controls, mutes, and de-emphasis facilities.

The device is available in a 48-pin TQFP package.

BLOCK DIAGRAM



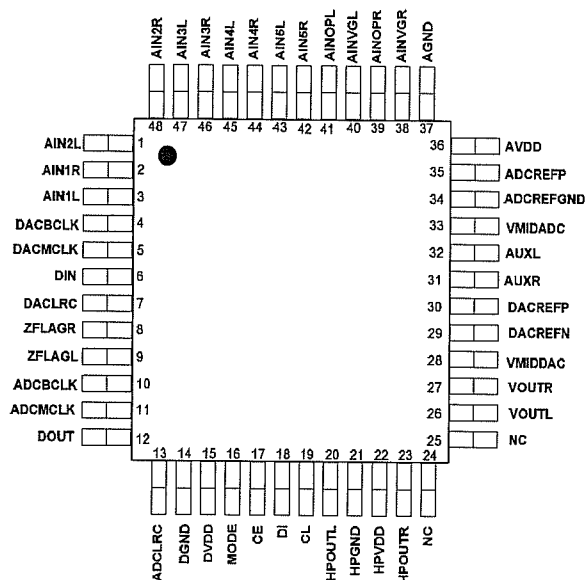
FEATURES

- Audio Performance
 - 108dB SNR ('A' weighted @ 48kHz) DAC
 - 102dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 32kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- Five stereo ADC inputs with analogue gain adjust from +24dB to –21dB in 0.5dB steps
- Programmable Limiter or Automatic Level Control (ALC)
- Stereo DAC with independent analogue and digital volume controls
- Stereo Headphone and Line Output
- 3-Wire SPI Compatible or 2-Wire Software Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
 - I²S, Left, Right Justified or DSP
 - 16/20/24/32 bit Word Lengths
- Analogue Bypass Path Feature
- Selectable AUX input to the volume controls
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation

APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- DVD-RW

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8776EFT/V	-25 to +85°C	48-pin TQFP	MSL2	240°C
WM8776EFT/RV	-25 to +85°C	48-pin TQFP (tape and reel)	MSL2	240°C
WM8776SEFT/V	-25 to +85°C	48-pin TQFP (lead free)	MSL2	260°C
WM8776SEFT/RV	-25 to +85°C	48-pin TQFP (lead free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AIN2L	Analogue Input	Channel 2 left input multiplexor virtual ground
2	AIN1R	Analogue Input	Channel 1 right input multiplexor virtual ground
3	AIN1L	Analogue Input	Channel 1 left input multiplexor virtual ground
4	DACBCLK	Digital input/output	DAC audio interface bit clock
5	DACMCLK	Digital input	Master DAC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
6	DIN	Digital Input	DAC data input
7	DACLRC	Digital input/output	DAC left/right word clock
8	ZFLAGR	Open Drain output	DAC Right Zero Flag output (external pull-up resistor required)
9	ZFLAGL	Open Drain output	DAC Left Zero Flag output (external pull-up resistor required)
10	ADCBCLK	Digital input/output	ADC audio interface bit clock
11	ADCCLK	Digital input	ADC audio interface master clock
12	DOUT	Digital output	ADC data output
13	ADCLRC	Digital input/output	ADC left/right word clock
14	DGND	Supply	Digital negative supply
15	DVDD	Supply	Digital positive supply
16	MODE	Digital input	Control interface mode select (5V tolerant)
17	CE	Digital input	Serial interface Latch signal (5V tolerant)
18	DI	Digital input	Serial interface data (5V tolerant)
19	CL	Digital input	Serial interface clock (5V tolerant)
20	HPOUTL	Analogue Output	Headphone left channel output
21	HPGND	Supply	Headphone negative supply
22	HPVDD	Supply	Headphone positive supply
23	HPOUTR	Analogue Output	Headphone right channel output
24	NC	Not bonded	
25	NC	Not bonded	
26	VOUTL	Analogue output	DAC channel left output
27	VOUTR	Analogue output	DAC channel right output
28	VMIDDAC	Analogue output	DAC midrail decoupling pin ; 10uF external decoupling
29	DACREFN	Analogue input	DAC negative reference input
30	DACREFP	Analogue input	DAC positive reference input
31	AUXR	Analogue input	DAC mixer right channel input
32	AUXL	Analogue input	DAC mixer left channel input
33	VMIDADC	Analogue Output	ADC midrail divider decoupling pin; 10uF external decoupling
34	ADCREFGND	Supply	ADC negative supply and substrate connection
35	ADCREFP	Analogue Output	ADC positive reference decoupling pin; 10uF external decoupling
36	AVDD	Supply	Analogue positive supply
37	AGND	Supply	Analogue negative supply and substrate connection
38	AINVGR	Analogue Input	Right channel multiplexor virtual ground
39	AINOPR	Analogue Output	Right channel multiplexor output
40	AINVGL	Analogue Input	Left channel multiplexor virtual ground
41	AINOPL	Analogue Output	Left channel multiplexor output
42	AIN5R	Analogue Input	Channel 5 right input multiplexor virtual ground
43	AIN5L	Analogue Input	Channel 5 left input multiplexor virtual ground
44	AIN4R	Analogue Input	Channel 4 right input multiplexor virtual ground
45	AIN4L	Analogue Input	Channel 4 left input multiplexor virtual ground
46	AIN3R	Analogue Input	Channel 3 right input multiplexor virtual ground
47	AIN3L	Analogue Input	Channel 3 left input multiplexor virtual ground
48	AIN2R	Analogue Input	Channel 2 right input multiplexor virtual ground

Note : Digital input pins have Schmitt trigger input buffers and pins 16, 17, 18 and 19 are 5V tolerant.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs (DI, CL, CE and MODE)	DGND -0.3V	+7V
Voltage range digital inputs (MCLK, DIN, ADCLRC, DACLRC, ADCBCLK and DACBCLK)	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T _A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Notes:

- Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, HPVDD, DACREFP		2.7		5.5	V
Ground	AGND, DGND, DACREFN, ADCREFGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, f_s = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V _{IL}				0.8	V
Input HIGH level	V _{IH}		2.0			V
Output LOW	V _{OL}	I _{OL} =1mA			0.1 x DVDD	V
Output HIGH	V _{OH}	I _{OH} =1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V _{V_{MID}}			AVDD/2		V
Potential divider resistance	R _{V_{MID}}			50k		Ω
DAC Performance (Load = 10k Ω, 50pF)						
0dBfs Full scale output voltage				1.0 x AVDD/5		V _{rms}
SNR (Note 1,2)		A-weighted, @ f _s = 48kHz		108		dB
SNR (Note 1,2)		A-weighted @ f _s = 96kHz		108		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input		108		dB
Total Harmonic Distortion (THD)		1kHz, 0dBfs		-97	-90	dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Headphone Buffer						
Maximum Output voltage				0.9		V _{rms}
Max Output Power (Note 4)	P _o	R _L = 32 Ω		25		mW
		R _L = 16 Ω		50		mW
SNR (Note 1,2)		A-weighted	85	92		dB
Headphone analogue Volume Gain Step Size			0.5	1	1.5	dB
Headphone analogue Volume Gain Range		1kHz Input	-73		+6	dB
Headphone analogue Volume Mute Attenuation		1kHz Input, 0dB gain		100		dB
Total Harmonic Distortion +Noise	THD+N	1kHz, R _L = 32Ω @ P _o = 10mW rms		-80 0.01	-60 0.1	dB %
		1kHz, R _L = 32Ω @ P _o = 20mW rms		-77 0.014	-40 1.0	dB %
Power Supply Rejection Ratio	PSRR	20Hz to 20kHz, without supply decoupling		-40		dB
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		V _{rms}
SNR (Note 1,2)		A-weighted, 0dB gain @ f _s = 48kHz		102		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ f _s = 96kHz 64 x OSR		100		dB
Dynamic Range (note 2)		A-weighted, -60dB full scale input		102		dB
Total Harmonic Distortion (THD)		1kHz, 0dBfs		-90	-80	DB

Test ConditionsAVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, f_s = 48kHz, MCLK = 256fs unless otherwise stated.

		1kHz, -3dBFS		-95	-85	dB
ADC Channel Separation		1kHz Input		90		dB
Programmable Gain Step Size			0.25	0.5	0.75	dB
Programmable Gain Range (Analogue)		1kHz Input	-21		+24	dB
Programmable Gain Range (Digital)		1kHz Input	-103		-21.5	dB
Mute Attenuation (Note 6)		1kHz Input, 0dB gain		76		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Analogue input (AIN) to Analogue output (VOUT) (Load=10k Ω, 50pF, gain = 0dB) Bypass Mode						
0dB Full scale output voltage				1.0 x AVDD/5		V _{rms}
SNR (Note 1)			90	100		dB
THD		1kHz, 0dB		-90		dB
		1kHz, -3dB		-95		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Mute Attenuation		1kHz, 0dB		100		dB
Supply Current						
Analogue supply current		AVDD = 5V		48		mA
Digital supply current		DVDD = 3.3V		8		mA

Notes:

- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
- All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
- VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
- Harmonic distortion on the headphone output decreases with output power.
- All performance measurement done using certain timings conditions (Please refer to section 'Digital Audio Interface').
- A better MUTE Attenuation can be achieved if the ADC gain is set to minimum.

TERMINOLOGY

- Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
- Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB = -32dB, DR = 92dB).
- THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
- Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
- Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
- Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

Product Specification

**SPECIFICATION
FOR
APPROVAL**

- Preliminary Specification
- Final Specification

Title	37.0" WXGA TFT LCD
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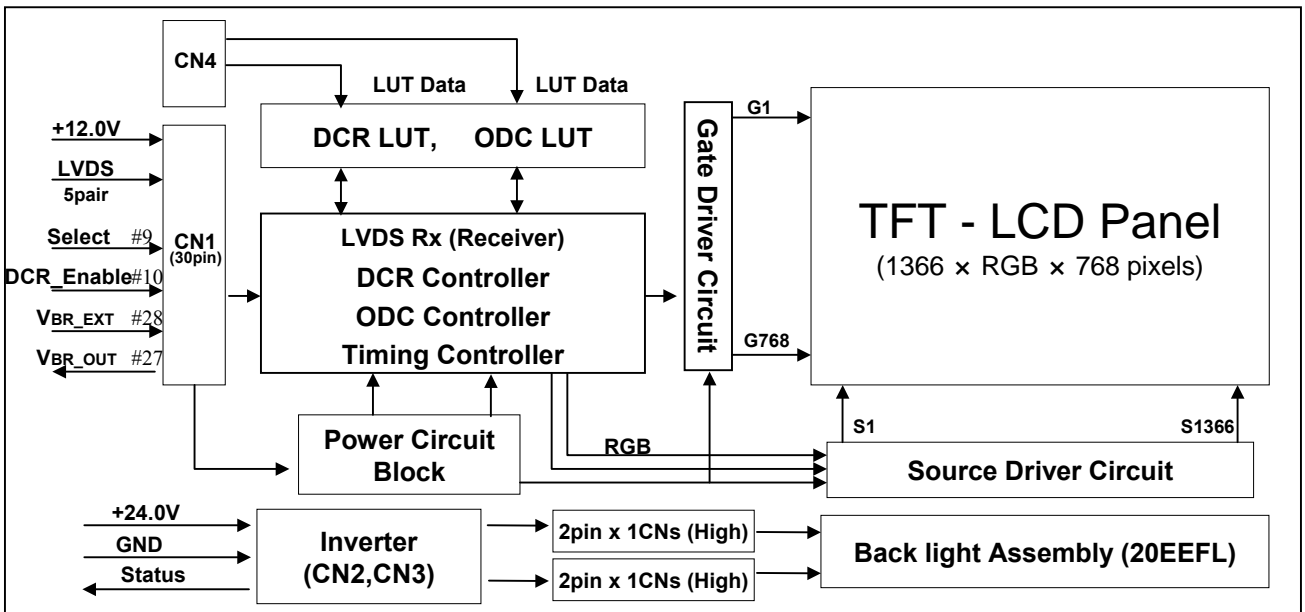
Product Specification

1. General Description

LC370WX1 is a Color Active Matrix Liquid Crystal Display with an integral External Electrode Fluorescent Lamp(EEFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 37.02 inch diagonally measured active display area with WXGA resolution (768 vertical by 1366 horizontal pixel array) Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus presenting a palette of more than 16.7M(true) colors.

It has been designed to apply the 8-bit 1 port LVDS interface.

It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	37.02 inches(940.3mm) diagonal
Outline Dimension	877.0mm(H) x 516.8mm(V) x 55.5mm(D) (Typ.)
Pixel Pitch	0.200mm x 0.600mm x RGB
Pixel Format	1366 horiz. by 768 vert. pixels RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors
Luminance, White	500 cd/m ² (Center 1 point Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178(Typ.), U/D 178(Typ.))
Power Consumption	Total 126Watt (Typ.) (Logic=4.8W, B/L=120W [$I_{LAMP}=100mA$])
Weight	10,500g (Typ.)
Display Operating Mode	Transmissive mode, normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer

Product Specification

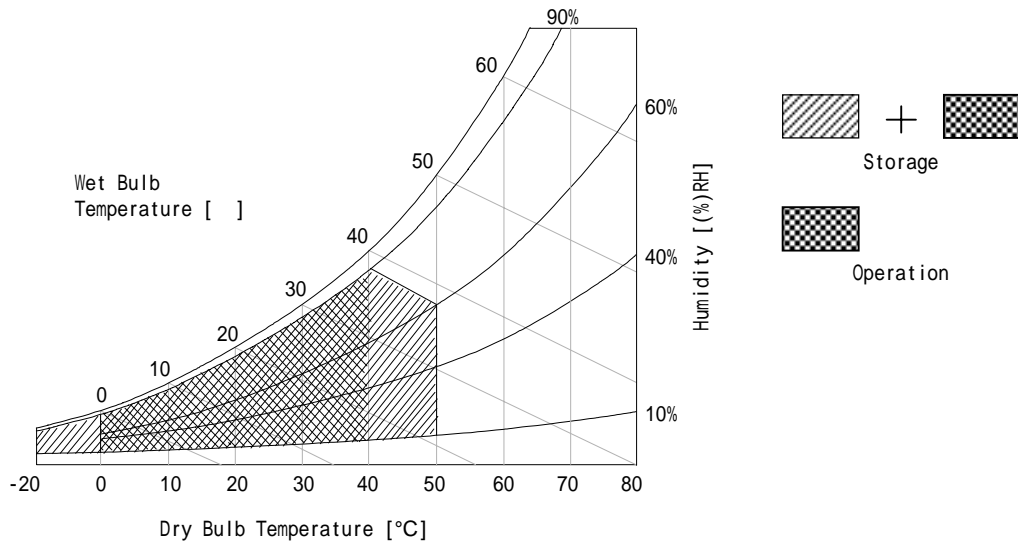
2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Remark
			Min	Max		
Power Input Voltage	LCM	VLCD	-0.3	14.0	VDC	at 25 ± 2 °C
	Backlight inverter	VBL	21.6	27.0	VDC	When operating
Option Input Voltage		VI	-0.3	3.6	VDC	DCR-Enable, Select
ON/OFF Control Voltage		VON/OFF	-0.30	5.25	VDC	
Brightness Control Voltage		VBr	0.0	3.3	VDC	
Operating Temperature		TOP	0	40		Note 1
Storage Temperature		TST	-20	50		
Operating Ambient Humidity		HOP	10	90	%RH	
Storage Humidity		HST	10	90	%RH	

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 °C Max. and no condensation of water.



Product Specification

3. Electrical Specifications

3-1. Electrical Characteristics

It requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The other input power for the EEFL/Backlight is to power inverter.

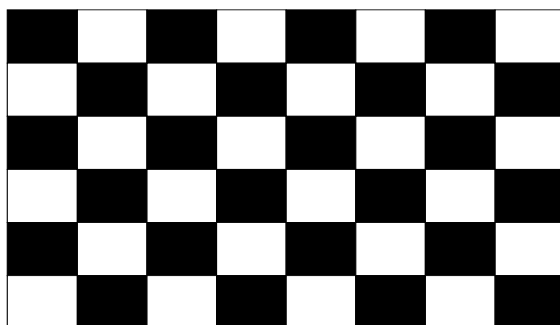
Table 2_1. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
MODULE :						
Power Input Voltage	VLCD	11.4	12.0	12.6	VDC	
Permissible Input Ripple Voltage	VRP	-	-	200	mVP-P	
Power Input Current	ILCD	-	400	500	mA	1
		-	535	785	mA	2
Option Input Voltage	High threshold	VIH	2.3	-	VDC	
	Low threshold	VIL	0	-	VDC	
Power Consumption	PLCD	-	4.8	6.0	Watt	1
Rush current	IRUSH	-	-	3.5	A	3

Note :

1. The specified current and power consumption are under the $V_{LCD}=12.0V$, $25 \pm 2^{\circ}C$, $f_v=60Hz$ condition whereas mosaic pattern(8 x 6) is displayed and f_v is the frame frequency.
2. The current is specified at the maximum current pattern.
3. The duration of rush current is about 2ms and rising time of power Input is 1ms(min.).

White : 255Gray
Black : 0Gray



Mosaic Pattern(8 x 6)

Product Specification

Table 2_2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note		
		Min	Typ	Max				
Inverter :								
Power Input Voltage	VBL	22.4	24.0	26.2	VDC	1		
Power Input Voltage Ripple		-	-	200	mVp-p			
Unloading Input Voltage				28.0	VDC			
Power Input Current	Operating	IBL	-	5.0	5.5	A	1	
	Turn on	IBL	-	5.5	6.0	A	1, 2	
Power Consumption	PBL	-	120	132	W	1		
Input Voltage for Control System Signals	Brightness Adjust		VBR	0		3.3	VDC	3
	On/Off	On	V on	2.50	5.00	5.25	VDC	
		Off	V off	-0.3	0.0	0.5	VDC	
Lamp :								
Life Time		50,000		-	Hrs	4		

Note :

- Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 120Min at $25 \pm 2^\circ\text{C}$ and $V_{BR} = 3.3\text{V}$.
The specified current and power consumption are under the typical supply Input voltage, 24.0V.
It is total power consumption.
LPL recommend Input Voltage is $24.0\text{V} \pm 5\%$.
(Philips system should keep the input voltage as $25.5\text{V} \pm 2\%$)
- It is not inrush current, it is the current at turn on time.
- Brightness Control.
This VBR Voltage control brightness.

VBR Voltage	Function
3.3V	Maximum Brightness (100%)
0V	Minimum Brightness.(20~30%)

- The life time is determined as the time at which luminance of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at $25 \pm 2^\circ\text{C}$.
Specified value is when lamp is aligned horizontally.

Product Specification

3-2. Interface Connections

This LCD employs two kinds of interface connection, a 30-pin connector is used for the module electronics and two 12-pin Connectors are used for the integral backlight system.

3-2-1. LCD Module

- LCD Connector(CN1) : FI-X30SSL-HF (Manufactured by JAE) or Equivalent
- Mating Connector : FI-X30C2L (Manufactured by JAE) or Equivalent

Table 3. MODULE CONNECTOR(CN1) PIN CONFIGURATION

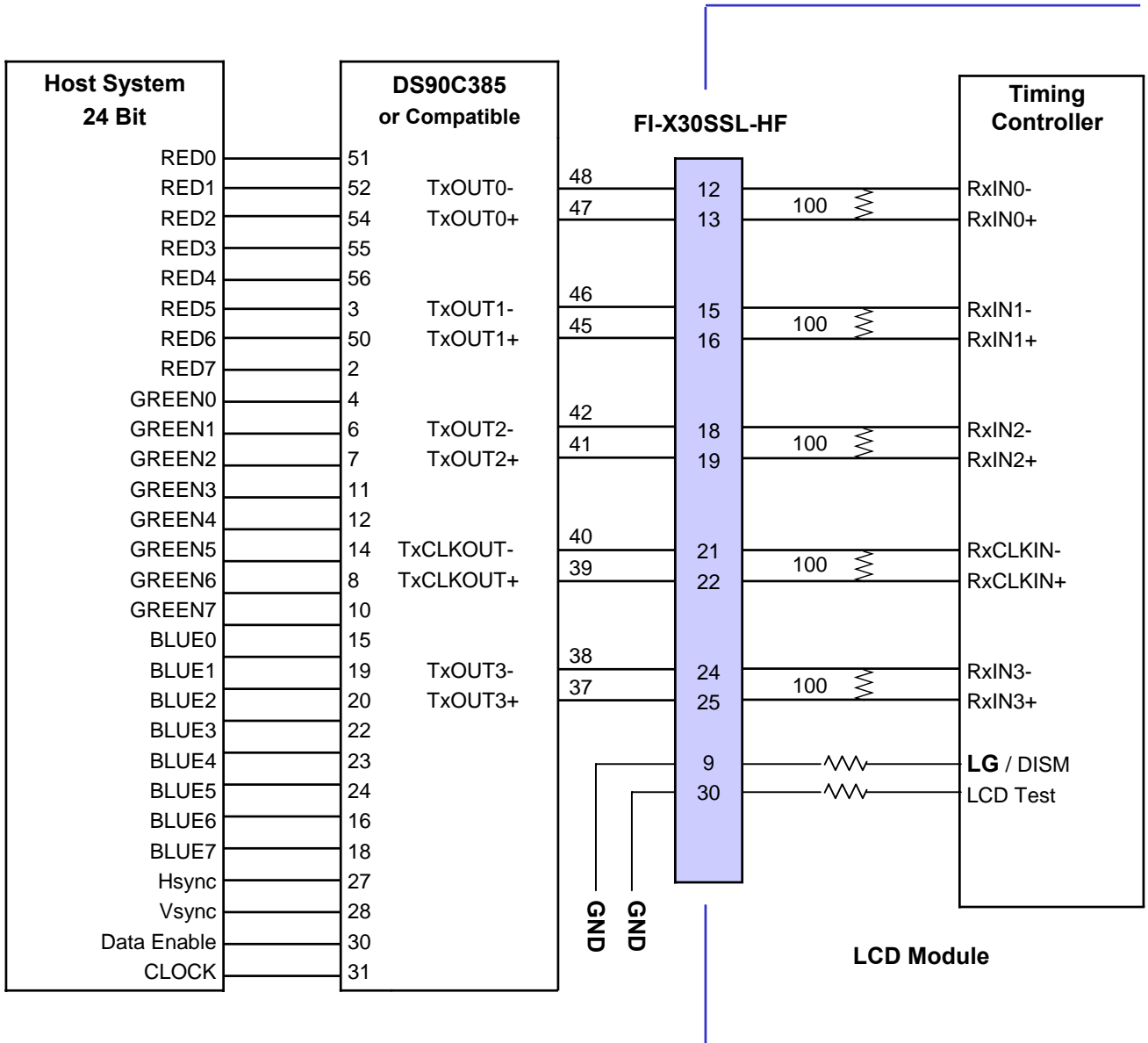
Pin No.	Symbol	Description	Note
1	VLCD	Power Supply +12.0V	
2	VLCD	Power Supply +12.0V	
3	VLCD	Power Supply +12.0V	
4	VLCD	Power Supply +12.0V	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	Select	Select LVDS Data format	1
10	DCR Enable	Dynamic CR Enable ('L' = Disable , 'H' = Enable)	2
11	GND	Ground	
12	RA-	LVDS Receiver Signal(-)	
13	RA+	LVDS Receiver Signal(+)	
14	GND	Ground	
15	RB-	LVDS Receiver Signal(-)	
16	RB+	LVDS Receiver Signal(+)	
17	GND	Ground	
18	RC-	LVDS Receiver Signal(-)	
19	RC+	LVDS Receiver Signal(+)	
20	GND	Ground	
21	RCLK-	LVDS Receiver Clock Signal(-)	
22	RCLK+	LVDS Receiver Clock Signal(+)	
23	GND	Ground	
24	RD-	LVDS Receiver Signal(-)	
25	RD+	LVDS Receiver Signal(+)	
26	GND	Ground	
27	VBR_OUT	VBR output form LCD module	
28	VBR_EXT	External VBR input from System to LCD module	
29	GND	Ground	
30	GND	Ground	3

Note: 1. If the pin no. 9 is Ground, Interface format is "LG", and if the pin no. 9 is Vcc(3.3V), Interface format is "DISM". See page 9 and 10.

2. This pin is pull down to the ground with 3kohm resistor in LCM.
If you want to enable DCR, contact this pin to VCC(3.3V) with 0ohm resistor.
For more information, see FIG 5 in the appendix 1.
3. The pin no. 30 is necessary for LCD test.
When LVDS signals are abnormal operation more than 3-Vsync times and power 12V is supplied,
'Open' or 'Vcc' : LCD operate itself some test patterns.(AGP – Auto Generation Pattern)
'Ground' : LCD operate itself a black pattern. (NSB – No Signal Black)
LPL recommend 'Ground' for NSB.
4. All GND (ground) pins should be connected together, which should be also connected to the LCD module's metal frame.
5. All VLCD (power input) pins should be connected together.
6. Input Levels of LVDS signals are based on the IEA 664 Standard.

Product Specification

Table 4. REQUIRED SIGNAL ASSIGNMENT FOR LVDS TRANSMITTER (Pin9="L" or "Open")



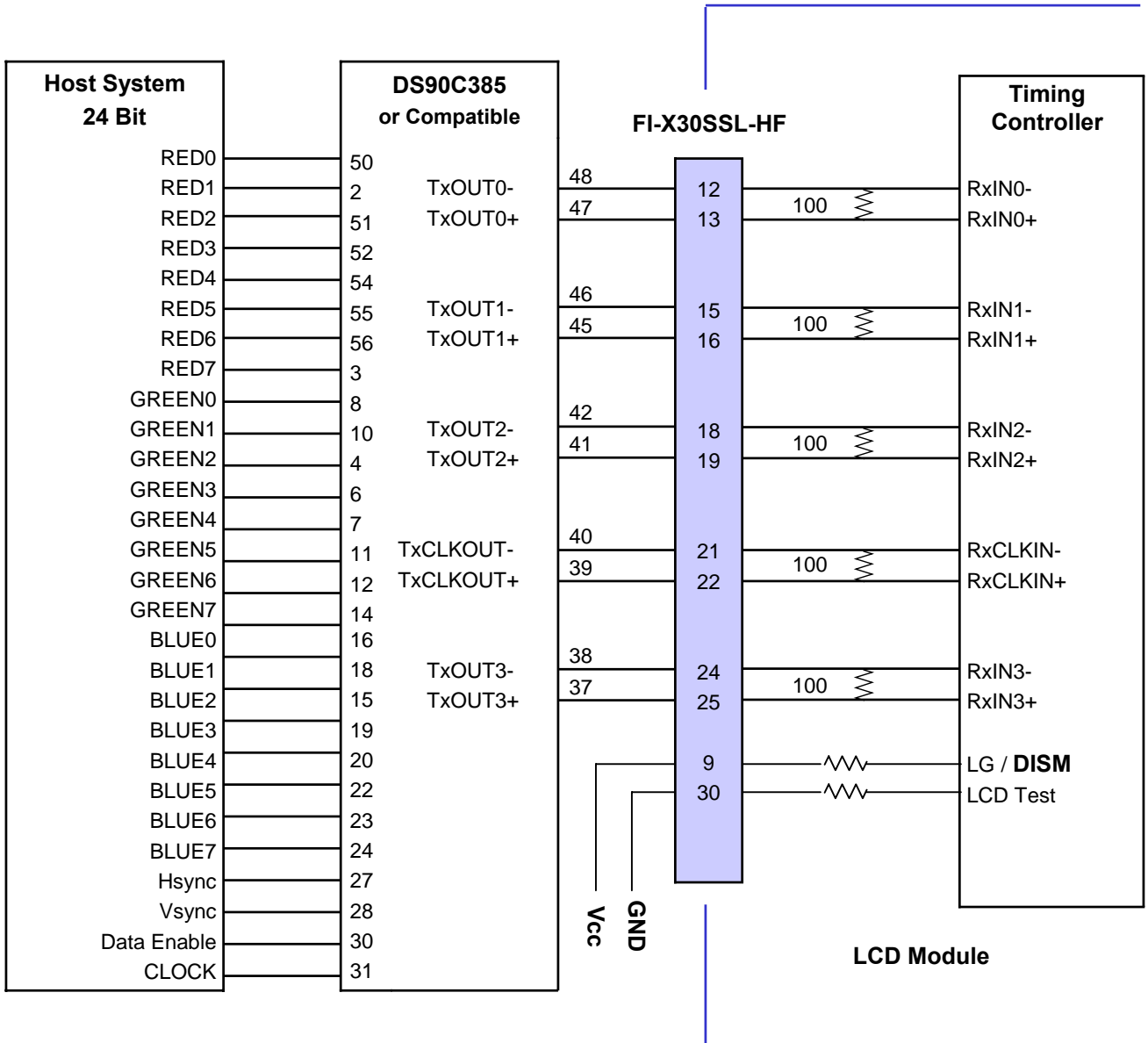
Note: 1. The LCD Module uses a 100 Ohm[] resistor between positive and negative lines of each receiver input.

2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (DS90C385 or Compatible)

3. '7' means MSB and '0' means LSB at R,G,B pixel data.

Product Specification

Table 5. REQUIRED SIGNAL ASSIGNMENT FOR LVDS TRANSMITTER (Pin9="H")



- Note: 1. The LCD Module uses a 100 Ohm[] resistor between positive and negative lines of each receiver input.
 2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (DS90C385 or Compatible)
 3. '7' means MSB and '0' means LSB at R,G,B pixel data.

Product Specification

3-2-2. Backlight Inverter

Input Connector

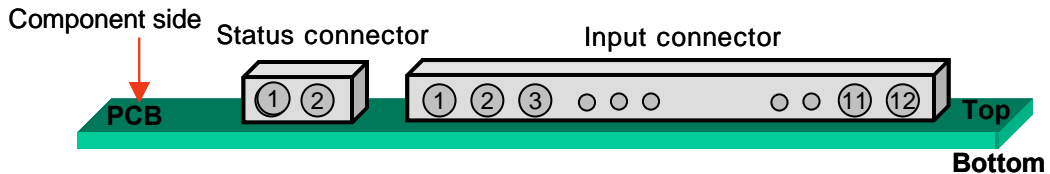
- Inverter Connector : S12B-PH-SM3(manufactured by JST) or Equivalent
- Mating Connector : PHR-12 or Equivalent

Status Connector

- Inverter Connector : 20022WR-02A00(manufactured by Yeon Ho co., Korea) or Equivalent
- Mating Connector : 20022HR-02S00(manufactured by Yeon Ho co., Korea) or Equivalent

Table 6. INVERTER CONNECTOR PIN CONFIGURATION

Pin No	Symbol	Description	Master	Slave	Note
1	VBL	Power Supply +24.0V	VBL	VBL	
2	VBL	Power Supply +24.0V	VBL	VBL	
3	VBL	Power Supply +24.0V	VBL	VBL	
4	VBL	Power Supply +24.0V	VBL	VBL	
5	VBL	Power Supply +24.0V	VBL	VBL	
6	GND	POWER GND	GND	GND	
7	GND	POWER GND	GND	GND	
8	GND	POWER GND	GND	GND	1
9	GND	POWER GND	GND	GND	
10	GND	POWER GND	GND	GND	
11	VBR	0V ~ 3.3V	VBR	Don't care	2
12	On/Off	0V ~ 5.0V	On/Off	Don't care	3
Option Pin(Lamp Open Status Detection)					
1	GND	POWER GND	GND		
2	Status	Upper 3.0V(Normal), Under 0.5V(Abnormal)	Status		



Note : 1. GND should be connected to the LCD module's metal frame.

- 2. Minimum Brightness : VBR = 0.0V
Maximum Brightness : VBR = 3.3V
- 3. VON : 2.5 ~ 5.0V
VOFF : -0.3 ~ 0.5V

Product Specification

3-3. Signal Timing Specifications

This is the signal timing required at the input of LVDS Transmitter. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

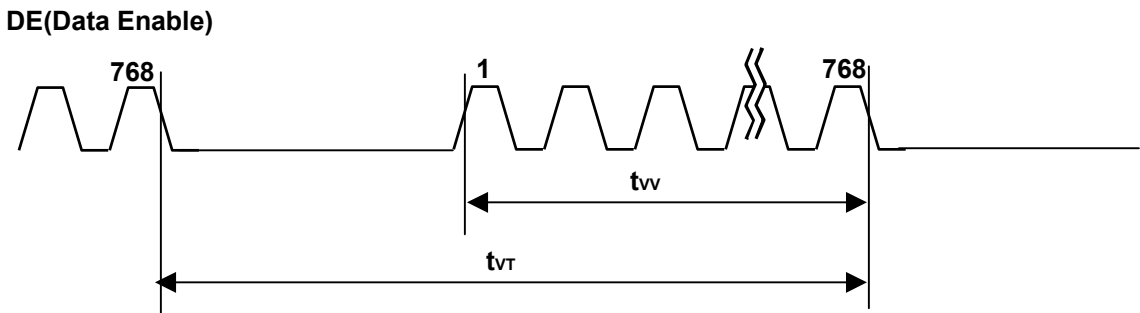
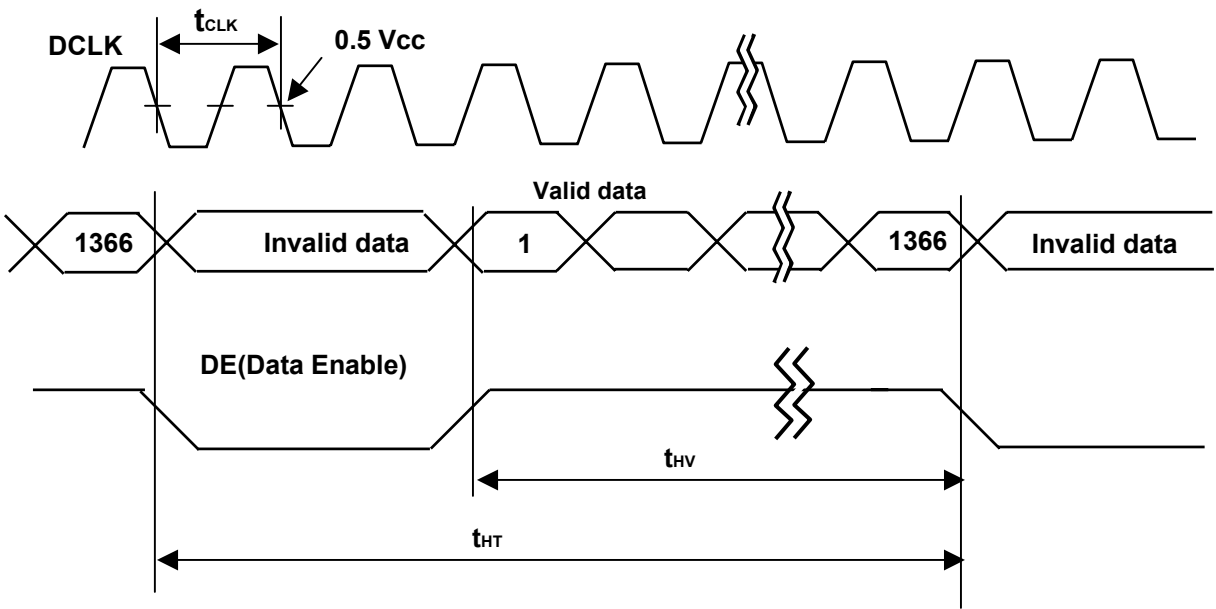
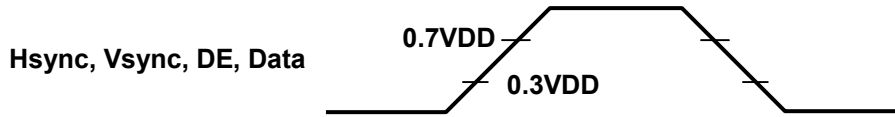
Table 7. TIMING TABLE (DE only Mode)

ITEM		Symbol	Min.	Typ.	Max.	Unit	Note
Clock	Frequency	f_{CLK}	68	72.3	80	MHz	
Hsync	Frequency	f_H	45	47.4	50	KHZ	
	Display Valid	t_{HV}	1366	1366	1366	Clks	
	Blank	$t_{HT}-t_{HV}$	140	162	410	Clks	
	Total	t_{HT}	1472	1528	1776	Clks	
Vsync	Frequency	f_V	47	60	63	HZ	PAL : 47~53Hz, NTSC : 57~63Hz
	Display Valid	t_{VV}	768	768	768	Lines	
	Blank	$t_{VT}-t_{VV}$	8	22	295	Lines	
	Total	t_{VT}	776	790	1063	Lines	

Notes:

1. The performance of the electro-optical characteristics are may be influenced by variance of the vertical refresh rates.
2. Above timing table is only valid for DE Mode.

3-4. Signal Timing Waveforms



Product Specification

3-5. Color Data Reference

The brightness of each primary color(red,green,blue) is based on the 8-bit gray scale data input for the color the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 8. COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB				LSB				MSB				LSB				MSB				LSB			
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							
	RED (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
							
	GREEN (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
							
	BLUE (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Product Specification

3-6. Power Sequence

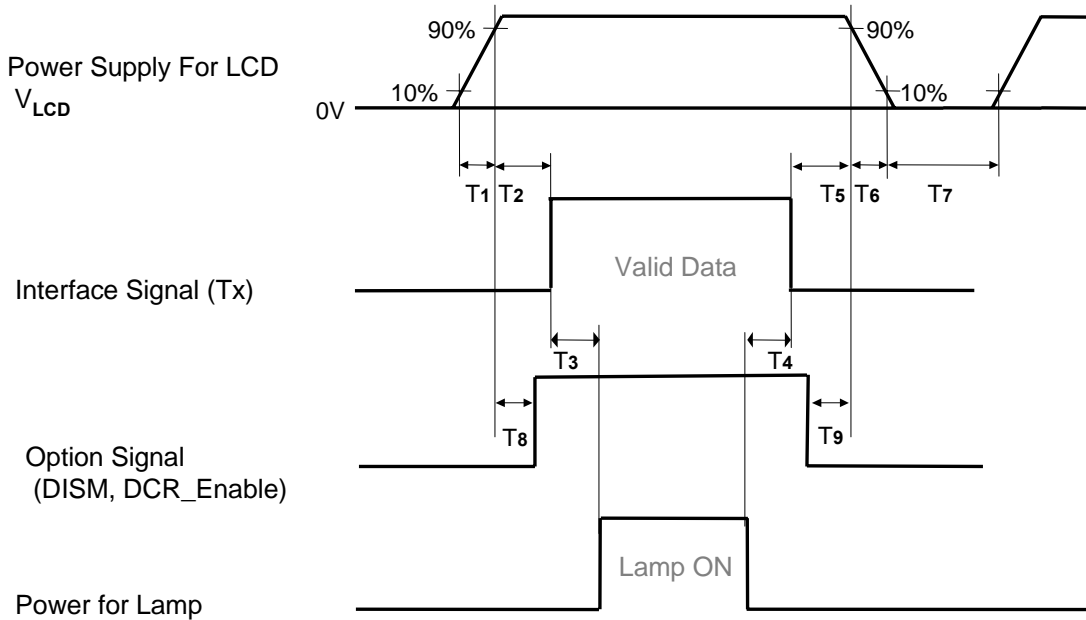


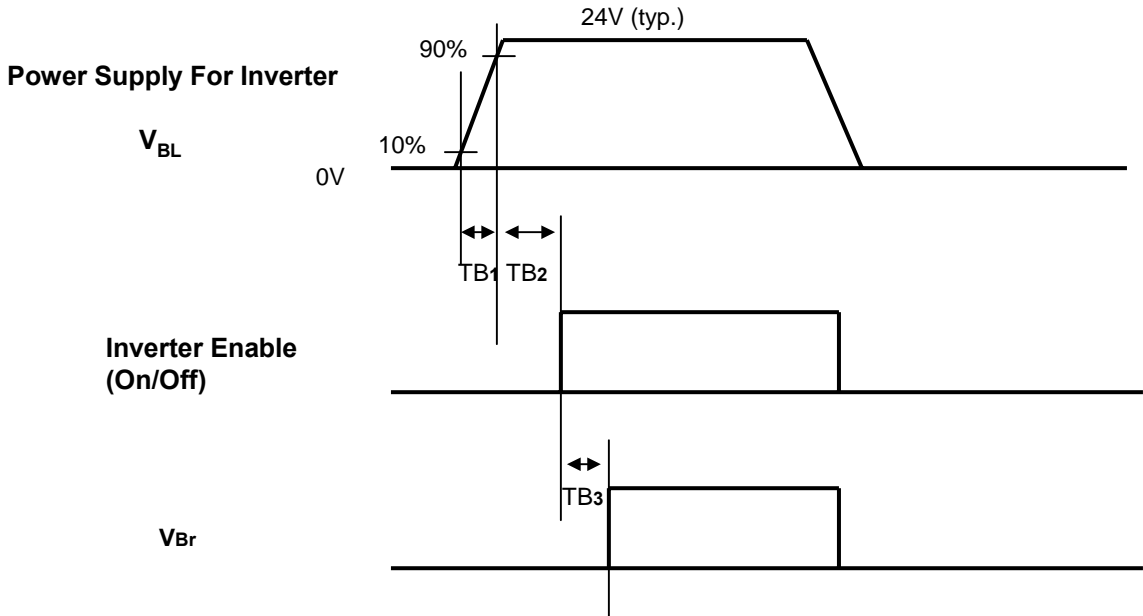
Table 9. POWER SEQUENCE

Parameter	Value			Unit
	Min	Typ	Max	
T1	1.0	-	20	ms
T2	5.0	-	50	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0.5	-	50	ms
T6	-	-	300	ms
T7	2.0	-	-	s
T8	0 < T8 < T2			ms
T9	0 < T9 < T5			ms

- Note :
1. Please avoid floating state of interface signal at invalid period.
 2. When the interface signal is invalid, be sure to pull down the power supply V_{LCD} to 0V.
 3. The case when the T2/T5 exceed maximum specification, it operates protection pattern(Black pattern) till valid signal inputted. There is no reliability problem.
 4. The T3/T4 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem.
 5. If the on time of option signal(DISM or AI_Enable) precedes the on time of Power(V_{LCD}), check the LCD logic Power(V_{CC}) is under 0.8V, otherwise it will be happened abnormal display.

Product Specification

3-6-2. Power Sequence for Inverter



3-6-3. Deep condition for Inverter

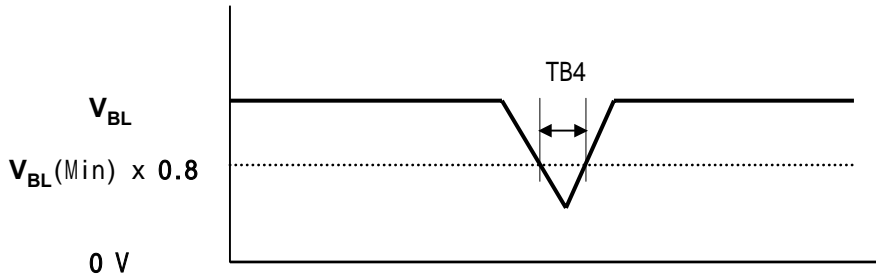


Table 10. POWER SEQUENCE FOR INVERTER

Parameter	Value			Unit	Remark
	Min	Typ	Max		
TB1	20	-	-	ms	After Inverter's connected
TB2	500	-	-	ms	
TB3	0	-	-	ms	
TB4	-	-	10	ms	$V_{BL(Min)} \times 0.8$

Note : TB1 describes rising time of 0V to 24V and is not applied at restarting time.
When the 24V Power is restart, the inverter enable signal must be restarted.

Product Specification

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' for 30min in a dark environment at $25 \pm 2^\circ\text{C}$. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0° .

It is presented additional information concerning the measurement equipment and method in FIG. 1.

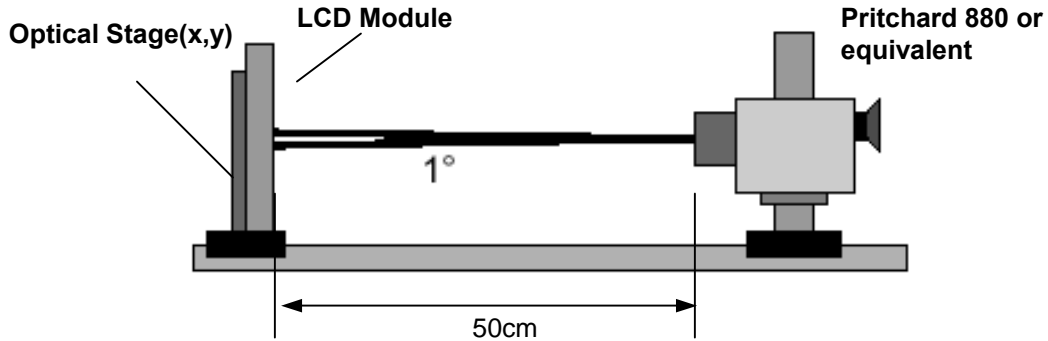


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 11. OPTICAL CHARACTERISTICS

$T_a = 25 \pm 2^\circ\text{C}$, $V_{LCD} = 12.0\text{V}$, $f_v = 60\text{Hz}$, $D_{clk} = 72\text{MHz}$, $V_{BR} = 3.3\text{V}$
Dynamic CR : Disabled

Parameter	Symbol	Value			Unit	Note	
		Min	Typ	Max			
Contrast Ratio	CR	600	800			1	
	CR _D (With AI)	1200	1600				
Surface Luminance, white	L _{WH}	400	500		cd/m ²	2	
Luminance Variation	δ_{WHITE} 5P			1.3		3	
Response Time	Gray to Gray	-	9	16	ms	4	
Color Coordinates [CIE1931]	RED	R _x	0.640	Typ +0.03			
		R _y	0.341				
	GREEN	G _x	0.287				
		G _y	0.610				
	BLUE	B _x	0.146				
		B _y	0.069				
	WHITE	W _x	0.285				
	W _y	0.293					
Viewing Angle (CR>10)							
	x axis, right($\phi=0^\circ$)	θ_r	85	89	-	degree	5
	x axis, left ($\phi=180^\circ$)	θ_l	85	89	-		
	y axis, up ($\phi=90^\circ$)	θ_u	85	89	-		
	y axis, down ($\phi=270^\circ$)	θ_d	85	89	-		
Gray Scale						6	

Product Specification

Notes 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at the center point(1).

CRD is measured when Dynamic CR is enabled.

2. Surface luminance is luminance value at the center point across the LCD surface 50cm from the surface with all pixels displaying white.
For more information, see FIG 2.

3. The variation in surface luminance , δ WHITE is defined as :

$$\delta \text{ WHITE}(5P) = \text{Maximum}(L_{on1}, L_{on2}, L_{on3}, \dots, L_{on5}) / \text{Minimum}(L_{on1}, L_{on2}, L_{on3}, \dots, L_{on5})$$

Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations .

For more information, see FIG 2.

4. Response time is the time required for the display to transition from G(N) to G(M) (Rise Time, Tr_R) and from G(M) to G(N) (Decay Time, Tr_D). For additional information see the FIG. 3. ($N < M$)

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information, see FIG 4.

6. Gray scale specification

Gamma Value is approximately 2.2.

For more information, see Table 12.

7. Black Level and Black Uniformity :

This is only for the reference. Please refer to attached Appendix A for the details.

Table 12. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ) Without DCR	Luminance [%] (Typ) With DCR
L0	0.12	0.06
L15	0.32	0.28
L31	1.10	0.96
L47	2.60	2.10
L63	4.90	4.10
L79	8.10	6.90
L95	12.1	10.3
L111	16.7	14.2
L127	21.6	19.5
L143	28.0	25.5
L159	35.4	33.0
L175	43.9	41.9
L191	53.3	51.3
L207	64.1	62.8
L223	75.8	74.5
L239	88.0	87.2
L255	100	100

Product Specification

Measuring point for surface luminance & measuring point for luminance variation

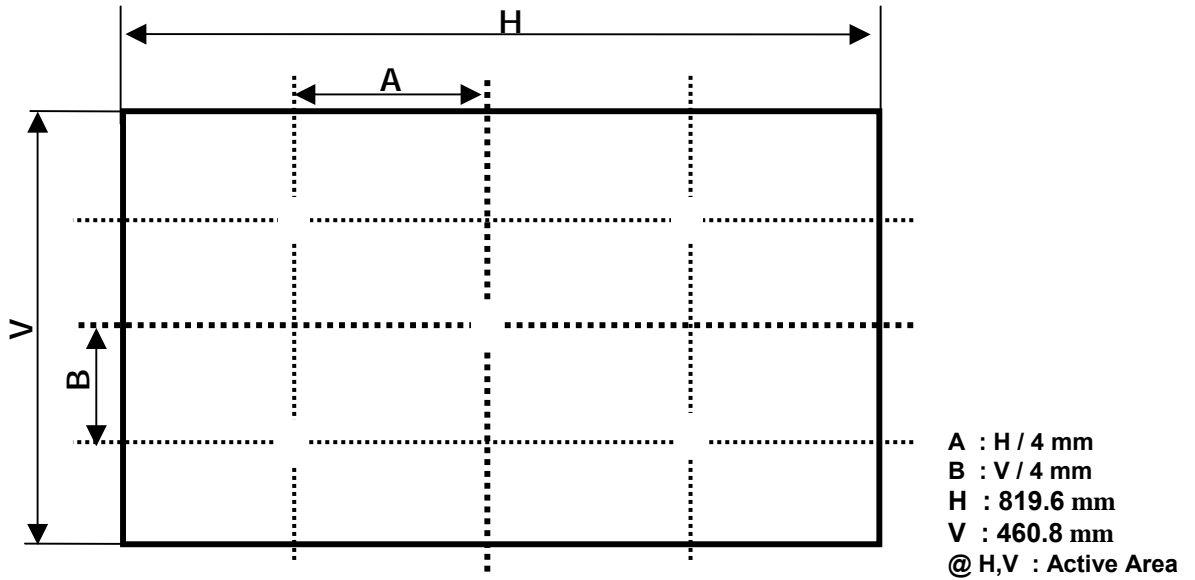


FIG. 2 Measure Point for Luminance

Response time is defined as the following figure and shall be measured by switching the input signal for “Gray(N)” and “Gray(M)”.

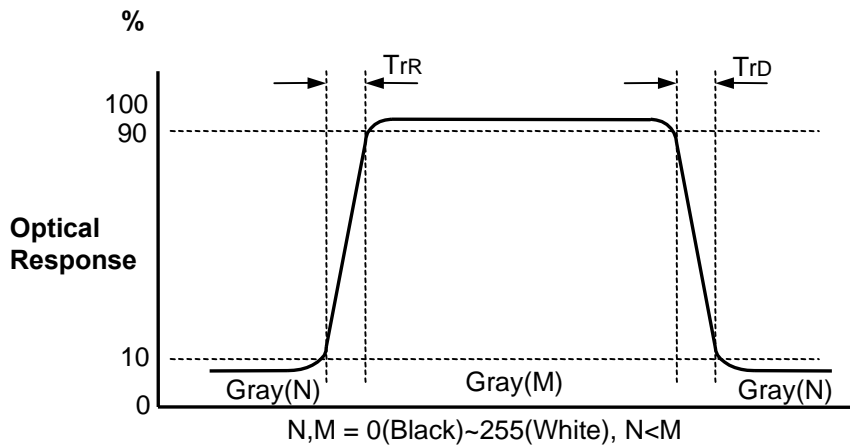


FIG. 3 Response Time

Product Specification

Dimension of viewing angle range

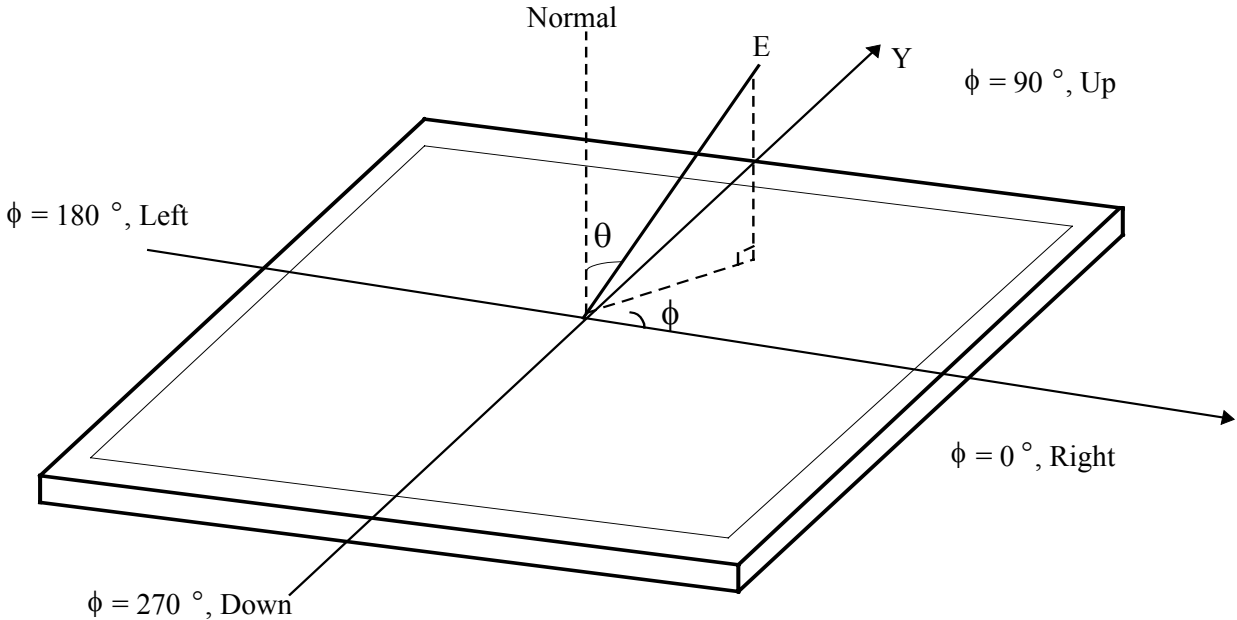


FIG. 4 Viewing angle

Product Specification

5. Mechanical Characteristics

The following items provide general mechanical characteristics. In addition the figures in the next page are detailed mechanical drawing of the LCD module.

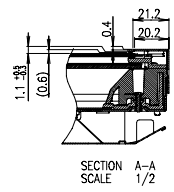
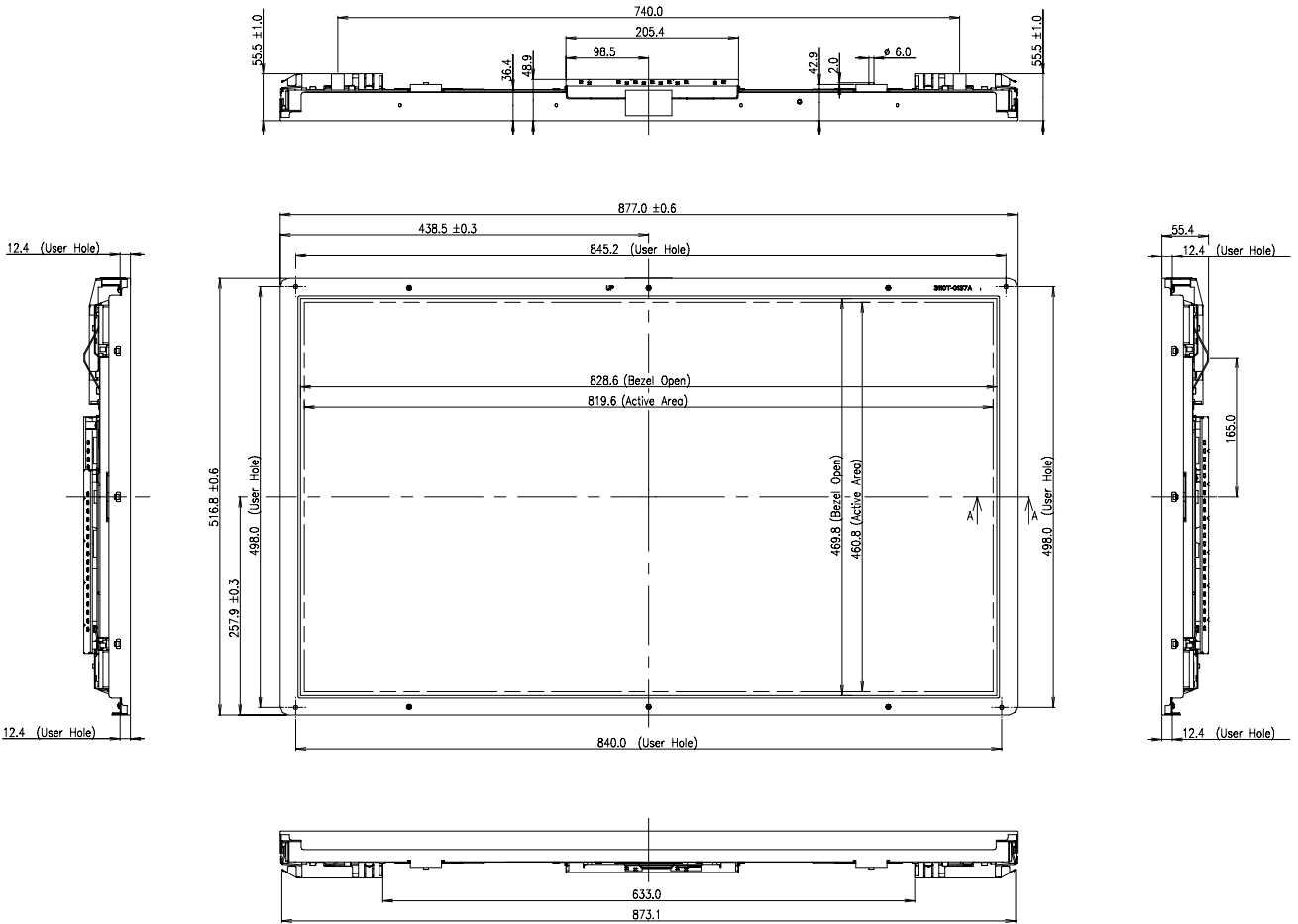
Table 13. MECHANICAL CHARACTERISTICS

Outline Dimension	Horizontal	877.0 mm
	Vertical	516.8 mm
	Depth	55.5 mm
Bezel Area	Horizontal	828.6mm
	Vertical	469.8mm
Active Display Area	Horizontal	819.6mm
	Vertical	460.8mm
Weight	10,500 (Typ.)/11,000(Max)	
Surface Treatment	Hard coating(3H) Anti-glare treatment of the front polarizer	

Note : Please refer to a mechanic drawing in terms of tolerance at the next page.

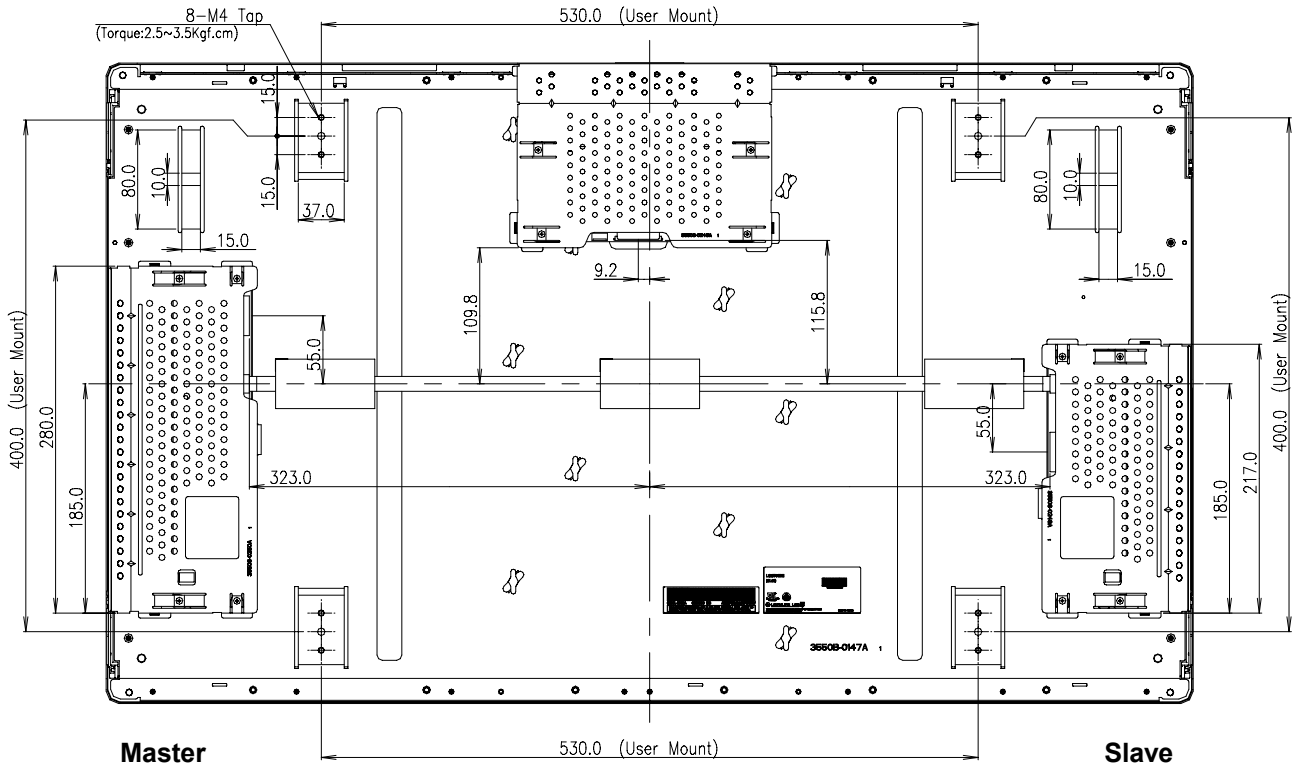
Product Specification

<FRONT VIEW>



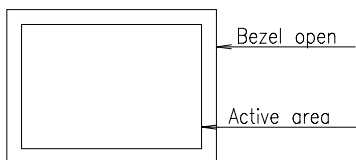
Product Specification

<REAR VIEW>



NOTES

1. Unspecified tolerances are to be $\pm 0.5\text{mm}$.
2. This drawing is only preliminary data and can be changed without previous notice.
3. Tilt and partial disposition tolerance of display area are as following.
 - (1) X-Direction : IA-BI $\leq 1.5\text{mm}$
 - (2) Y-Direction : IC-DI $\leq 1.5\text{mm}$



Product Specification

6. Reliability

Table 14. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 50°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 40°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (non-operating)	Wave form : random Vibration level : 1.0G RMS Bandwidth : 10-500Hz Duration : X,Y,Z, 10 min One time each direction
6	Shock test (non-operating)	Shock level : 100G Waveform : half sine wave, 2ms Direction : ± X, ± Y, ± Z One time each direction
7	Humidity condition Operation	Ta= 40 °C, 90%RH
8	Altitude operating storage / shipment	0 - 14,000 feet(4267.2m) 0 - 40,000 feet(12192m)

7. International Standards

7-1. Safety

- a) UL 60950-1:2003, First Edition, Underwriters Laboratories, Inc., Standard for Safety of Information Technology Equipment.
- b) CAN/CSA C22.2, No. 60950-1-03 1st Ed. April 1, 2003, Canadian Standards Association, Standard for Safety of Information Technology Equipment.
- c) EN 60950-1:2001, First Edition, European Committee for Electrotechnical Standardization(CENELEC) European Standard for Safety of Information Technology Equipment.

7-2. EMC

- a) ANSI C63.4 "Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. "American National Standards Institute(ANSI), 1992
- b) C.I.S.P.R. "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." International Special Committee on Radio Interference.
- c) EN 55022 "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." European Committee for Electrotechnical Standardization.(CENELEC), 1998 (Including A1: 2000)

Product Specification

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M
---	---	---	---	---	---	---	---	---	---	---	---	---

A,B,C : SIZE(INCH)
E : MONTH

D : YEAR
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011
Mark	1	2	3	4	5	6	7	8	9	0	1

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 5 pcs

b) Box Size : 973mm X 493mm X 577mm

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9-1. Mounting Precautions

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

9-2. Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
 $V = \pm 200\text{mV}$ (Over and under shoot voltage)
- (2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
- (7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
- (8) A screw which is fastened up the steels should be a machine screw.
(if not, it causes metallic foreign material and deal LCM a fatal blow)
- (9) Please do not set LCD on its edge.

Product Specification

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. Handling Precautions for Protection Film

- (1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

Appendix 1.

The figure of the DCR_ENABLE Circuit Block Diagram

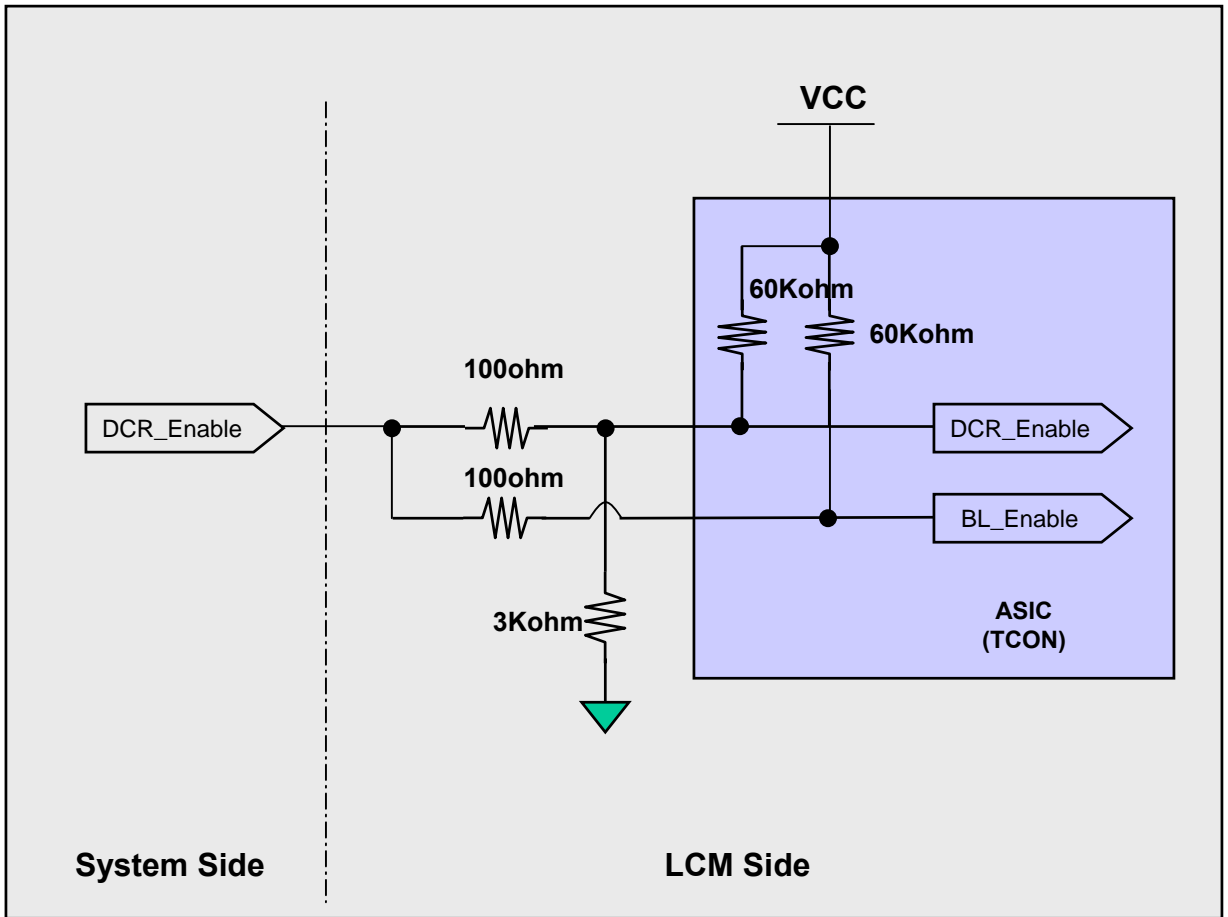
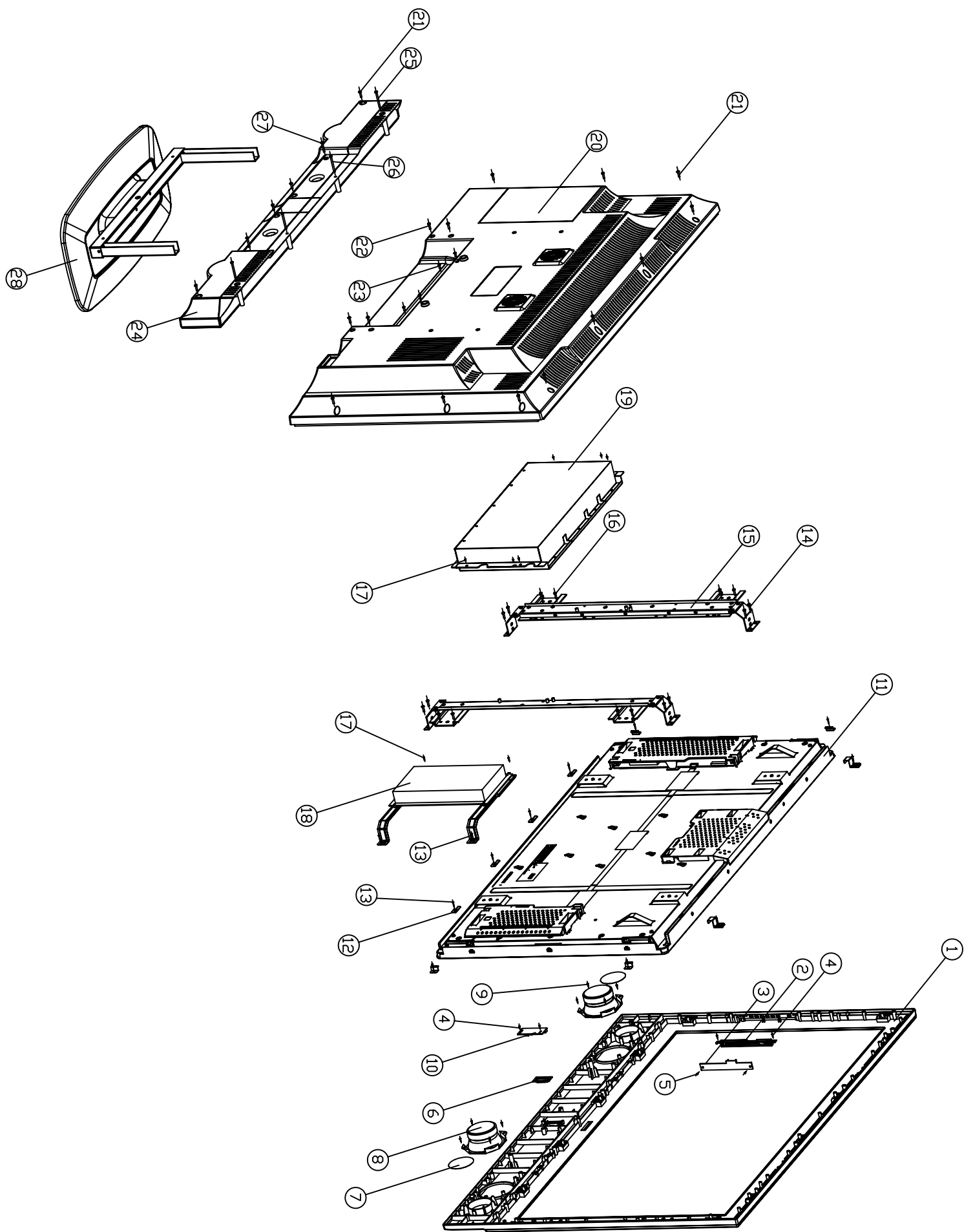


Fig.5 The DCR_ENABLE Circuit Block Diagram

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER , DO NOT UPDATE MASTER MANUALLY



DWG. REV.	ZONE	DESCRIPTION	DATE	REVISOR
		REL FOR TOOLING		LJ

ITEM	DESCRIPTION	TYPE	QTY	REMARK
28	BASE ASSY	ASSEMBLY	1	
27	TAPPING SCREW	PART	2	
26	TAPPING SCREW	PART	2	
25	TAPPING SCREW	PART	2	
24	SPEAKER CABINET BACK	PART	1	
23	MACH SCREW	PART	4	
22	MACH SCREW	PART	4	
21	TAPPING SCREW	PART	14	
20	BACK CABINET	ASSEMBLY	1	
19	MAIN BOARD ASSY	ASSEMBLY	1	
18	POWER ASSY	ASSEMBLY	1	
17	MACH SCREW	PART	8	
16	MACH SCREW	PART	8	
15	MAIN SUPORT	PART	2	
14	TAPPING SCREW	PART	8	
13	TAPPING SCREW	PART	12	
12	*2*BKT FRD PANEL	PART	10	
11	37' PANEL ASSY	ASSEMBLY	1	
10	REMOTE PCB	PART	1	
9	TAPPING SCREW	PART	8	
8	BURDDN SPEAKER	PART	2	
7	PVC SHEET	PART	2	
6	REMOTE LENS	PART	1	
5	TAPPING SCREW	PART	2	
4	TAPPING SCREW	PART	4	
3	FUNCTION KEY PCB ASSY	ASSEMBLY	1	
2	FUNCTION KEY	PART	1	
1	FRONT CABINET	PART	1	

DRAWN.	LJ	TOLERANCE UNLESS OTHERWISE SPECIFIED	KAWA ELECTRONIC R & D CENTRE
CHECKED		0: ±0.30	
		0.0 ±0.10	
APPRD.		0.00: ±0.05	
3rd ANGLE PROJECTION		ANGULAR: ±0.3°	
		UNIT : mm	

TITLE	LCT3785TA-EXP		
MODEL NO.	LCT37AD		
PART NO.	A3	DWG. NO.	LCT37ADAIAPS-C01
	LCT37ADAIAPS-C01		LCT37ADAIAPS-C01
SCALE 1:10	QTY. 1	SHEET 1	OF 1

Spare part list for LCT37SHA

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
	LCT37ADAIA1PS-C01	SCOTT LCT37AD(LCT37SHA) S-MT8202 LPL(LC370WX1-SL02 V1.0) HORIZONTAL AC120V/60HZ USA BLACK (RS)			
1>	510-L37SD03-04AK	FLAT CARTON BOX SCOTT LCT37SHA S-MT8202 LPL USA K	1.000000	Piece	K
2>	580-L37AD4A-07AP	IB E FOR SCOTT LCT37SHA TV+DTV W/ O PIP LPL S-MT8202 USA (RS)	1.000000	Piece	K
3>	E3407-081001	CORD FFC P0.5 50P L=110 B-0.5-50X110- 4(8)X4(8)-0.3X0.035	1.000000	Piece	K
4>	E7501-056105	REMOTE CONTROL K001 "SCOTT" 44KEYS S-MT8202 LCD TV USA BLACK	1.000000	SET	K
5>	E7801-P02003	PCB ASSY PSU BOARD MEGMEET MLT386X FOR 37LCD AC110-240V OUTPUT 12V/8V/24V 250W	1.000000	SET	K
6>	771EL37AD03-04	PCB ASS'Y MAIN S-MT8202 FOR LCT37" LPL	1.000000	SET	K
7>	771S42D102-02	ATSC TUNER PCB ASS'Y (MT5111CE) W/ O MAX3232	1.000000	SET	K
8>	200-L37AD21-06AA	CABINET FRONT BLACK LCT37SHA LPL PANEL USA A	1.000000	Piece	S
9>	202-L37AD05-01AA	CABINET BACK BLACK LCT37AD A	1.000000	Piece	S
10>	206-L37AD01-01R	SPEAKER BACK COVER BLACK	1.000000	Piece	S
11>	231-L32AD01-05AR	BASE COVER BLACK(SA-598)	1.000000	Piece	S
12>	277-L32AD11-06S	FUNCTION KEY BLACK(SA-598) S	1.000000	Piece	S
13>	300-L37AD0B-02C	POLYFOAM BOTTOM	1.000000	Piece	S
14>	300-L37AD0C-02C	POLYFOAM TOP	1.000000	Piece	S
15>	310-030404-01	POLYBAG 110MMX80MMX0.04MM	2.000000	Piece	S
16>	310-041204-01V	POLYBAG 4"X12"X0.04 AV	1.000000	Piece	S
17>	310-102004-01T	POLYBAG FOR 32" 37" METAL CROS SBEAM	1.000000	Piece	S
18>	310-111404-07V	POLYBAG 11"X14"X0.04 FV	1.000000	Piece	S

Spare part list for LCT37SHA

19>	310-142804-01T	POLYBAG FOR 32" 37" STAND T 14"X28"X0.04	1.000000	Piece	S
20>	310-444750-07V	POLYBAG 44X47X50	1.000000	Piece	S
21>	370-42D102-01	PAD CORD SPONG FOR SPK	1.000000	Piece	S
22>	370-L32AD01-01Y	RUBBER FOOT 20X6 L32AD Y	6.000000	Piece	S
23>	388-42SB04-01H	POWER PLATE SANSUI 42SB H	1.000000	Piece	S
24>	388-L37SD01-01H	PVC (94V0) SHEET FOR POWER PCB	1.000000	Piece	S
25>	389-L32AB01-01	PVC SHEET L32AB	2.000000	Piece	S
26>	420-L32AD11-01	BOTTOM PLATE	1.000000	Piece	S
27>	420-L37AD14-01S	MAIN SUPPORT "R"	1.000000	Piece	S
28>	426-L37AD02-01S	AC JACK BRACKET	1.000000	Piece	S
29>	429-L32AB13-01	L SHEET	2.000000	Piece	S
30>	429-L32AB56-01	"U" TOP CROSSBEAM LCT32AD	1.000000	Piece	S
31>	429-L32AD0E-01	SECURE LEG	2.000000	Piece	S
32>	429-L37AD0C-01S	POWER SUPPORT FOR LPL	2.000000	Piece	S
33>	429-L37AD0D-01	"Z" BKT FOR LPL	4.000000	Piece	S
34>	429-L37AD0E-01	"Z" BKT FOR LPL	4.000000	Piece	S
35>	436-L32AB0G-01S	TERMINAL SHEET FOR COMPONENT X2	1.000000	Piece	S
36>	481-L32AB06-01S	SHIELDING BOTTOM MT8202	1.000000	Piece	S
37>	483-L32AB32-01S	SHIELDING COVER	1.000000	Piece	S
38>	486-L37AD01-01	NAME PLATE SCOTT SIL/BLACK LCT37SHA	1.000000	Piece	S

Spare part list for LCT37SHA

39>	522-421D01-01	MASKING PAPER	1.000000	Piece	S
40>	560-L37AD01-04AP	MODEL LABEL SCOTT LCT37SHA S-MT8202 USA P	1.000000	Piece	S
41>	563-119-	SERIAL NO. LABEL	1.000000	Piece	S
42>	568-P46T02-02	WARNING LB ENG 42SF NIL	1.000000	Piece	S
43>	578-L37AD01-01AP	FUNCTION SHEET FOR TERMINAL LCT37" S-MT8202 USA P	1.000000	Piece	S
44>	579-42D102-09	SERIAL NO/BAR CODE LABEL 42D1	1.000000	Piece	S
45>	579-42D105-01	PROTECTIVE EARTH LABEL FOR ESA 42TD1	1.000000	Piece	S
46>	579-L27AD09-01	CAUTION LABEL ENG AKAI	1.000000	Piece	S
47>	579-L32AD09-02AP	FCC STATEMENT LABEL 77X20MM	1.000000	Piece	S
48>	579-L37AD01-06AP	BAR CODE LABEL SCOTT LCT37SHA USA P	2.000000	Piece	S
49>	590-L37AD01-06AP	WARRANTY CARD SCOTT ENG LCT37SHA USA P	1.000000	Piece	S
50>	593-L37AD01-06AP	SCOTT INSERTION CARD ENG LCT37SHA USA P	1.000000	Piece	S
51>	599-L37AD02-02BP	IB SHEET E FOR LCT37 STAND (SQUARE) USA (RS)	1.000000	Piece	S
52>	E3219-002003	EI I LET EMI FILTER WIT WIRES IOSSI-R-Q(B) HIGH&LOW	1.000000	Piece	S
53>	E3404-157004	AC CORD UL 1.88M (YY-3/ST3 YUNBIAO)	1.000000	Piece	S
54>	E3421-925118	WIRE ASSY 8P2.5/7P2.0 L170MM 5V 12V SIGNAL POWER MT8202	1.000000	Piece	S
55>	E3421-925127	WIRE ASSY TJC3-2Y L860 SPK-R MT8202	1.000000	Piece	S
56>	E3421-925139	WIRE ASSY TJC3-3Y L760MM LCD37" MT8202 SPK-L	1.000000	Piece	S
57>	E3421-925151	WIRE ASSY 16P/2.0/11P/2.5/10P/2.5/8P/2.0 FOR MT8202 5V/12V/9V	1.000000	Piece	S
58>	E3421-925153	WIRE ASSY 250MM 3WIRES 20# 1617 FOR POWER IN PUT	1.000000	Piece	S

Spare part list for LCT37SHA

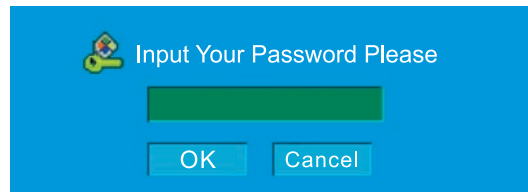
59>	E3421-926112	WIRE ASSY L=540 2.0/2.5 4P FOR 32LCD W/EMI	1.000000	Piece	S
60>	E3461-000121	WIRE ASSY P2.5 8P/P2.0 12P/P2.0 3P L780MM/L500MM /L300MM INVERTER MT8202 LPL	1.000000	Piece	S
61>	E3461-064042	WIRE ASSY 1H2.5-2H2.0 20099 L350 7P/5P FOR MT8202 37" STANDBY	1.000000	Piece	S
62>	E3471-000072	WIRE WS SHIELD FOR MT8202 MICO KEY 13P/8P+5P L650/L750MM W/O EMI	1.000000	Piece	S
63>	E3471-000086	WIRE WS SHIELD WIRE LCT37" L=220MM LPL MT8202 LVDS	1.000000	Piece	S
64>	E4801-124001	SPEAKER 8 OHM 10W D3" YD78-1	2.000000	Piece	S
65>	E6203-37PD01	DISPLAY LCD 37" LPL LC370WX1-SL02 V1.0	1.000000	Piece	S
66>	E7301-010002	BATTERY AAA R03P1.5V <2>	2.000000	Piece	S
67>	771BL27AD01-02	IR RECEIVE PCB ASS'Y FOR "ILO" LCD S-MT8202	1.000000	SET	S
68>	771KL37AD01-01	KEY PCB ASSY FOR LCT37AD	1.000000	SET	S

If you forget your V-Chip Password

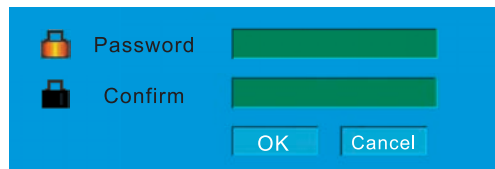
- Omnipotence V-Chip Password: 8202.

Using the “Change Password” item

- ❶ When enter the “V-Chip” menu, select “Change Password”.
- ❷ Press ▲ or ▼ button to highlight the “Change Password” item.
- ❸ Press **Enter** button to confirm and pop up a menu.



- ❹ Use 0~9 buttons input the omnipotence password (8202), then Press **Enter** button to enter and pop up a menu.



- ❺ Use 0~9 buttons input your new password.
- ❻ Press ▼ button to move to confirm blank.
- ❼ Use 0~9 buttons input your new password again.
- ❽ Press **Enter** button to confirm

-Suggest: Change to your familiar Password again.

Software Upgrade

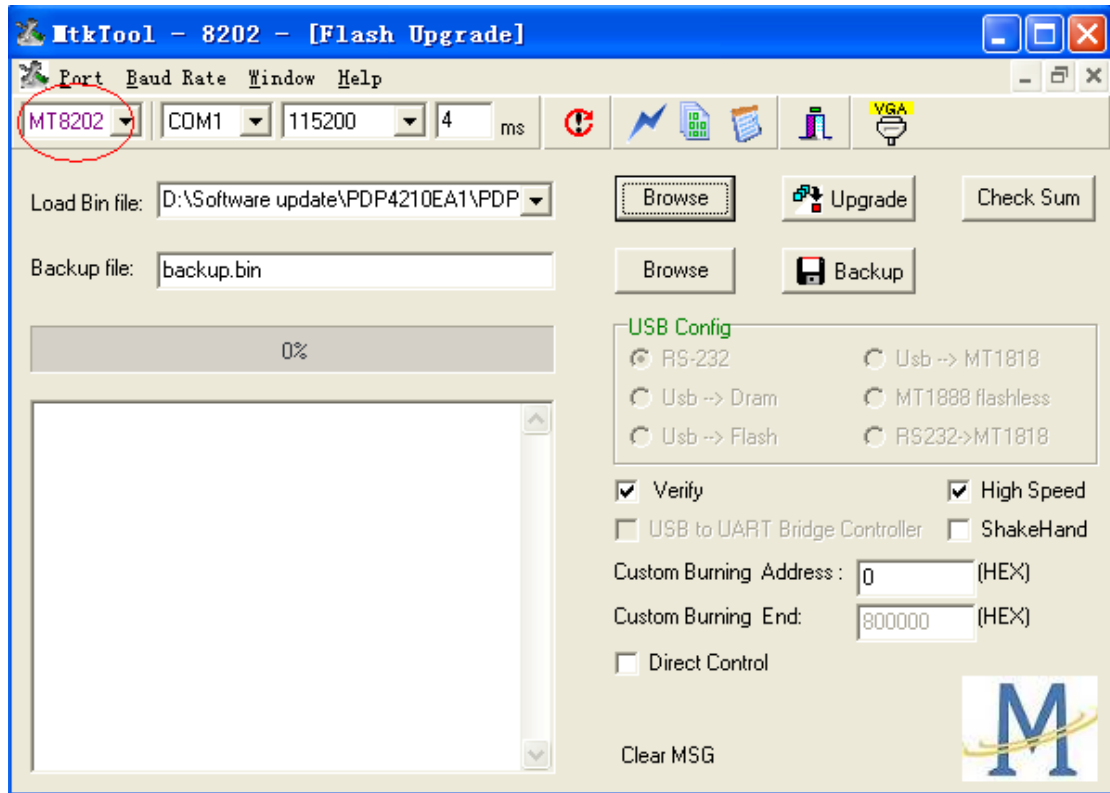
Process of update MT8202

Preparing :

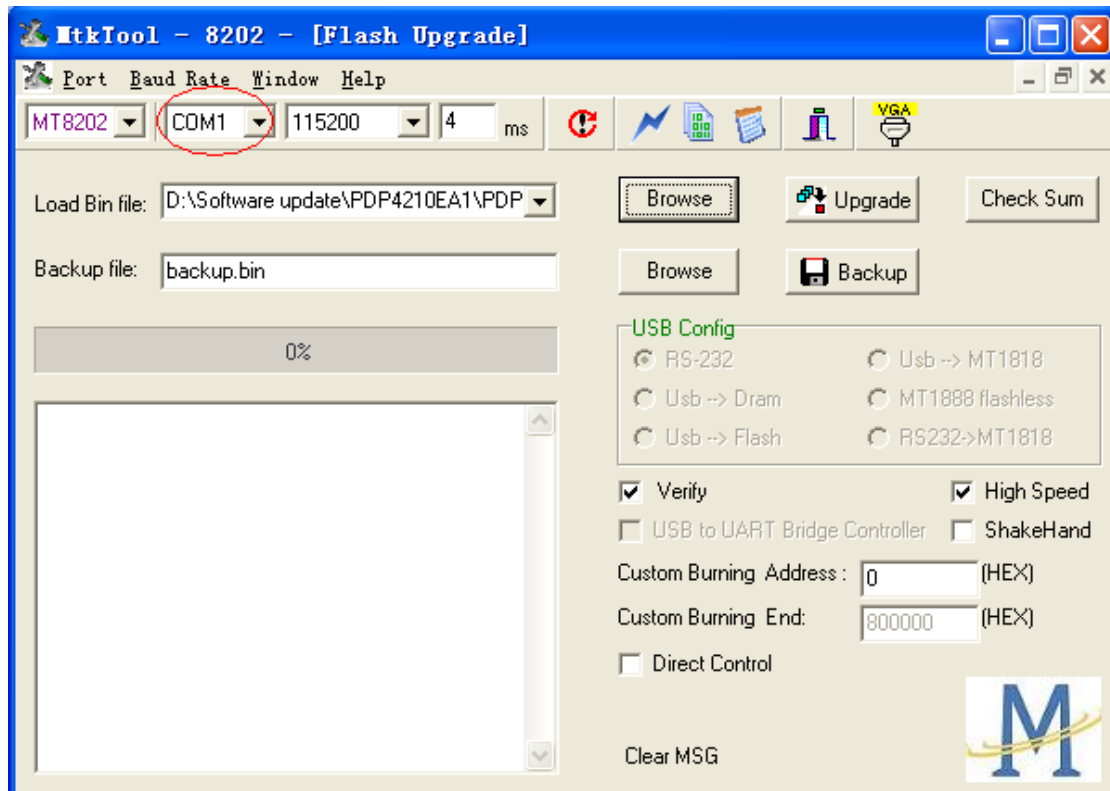
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**. Please find the details for connecting **referring to the appendix at the end of this file**.
2. Store the MtkTool into the PC .

Downloading :

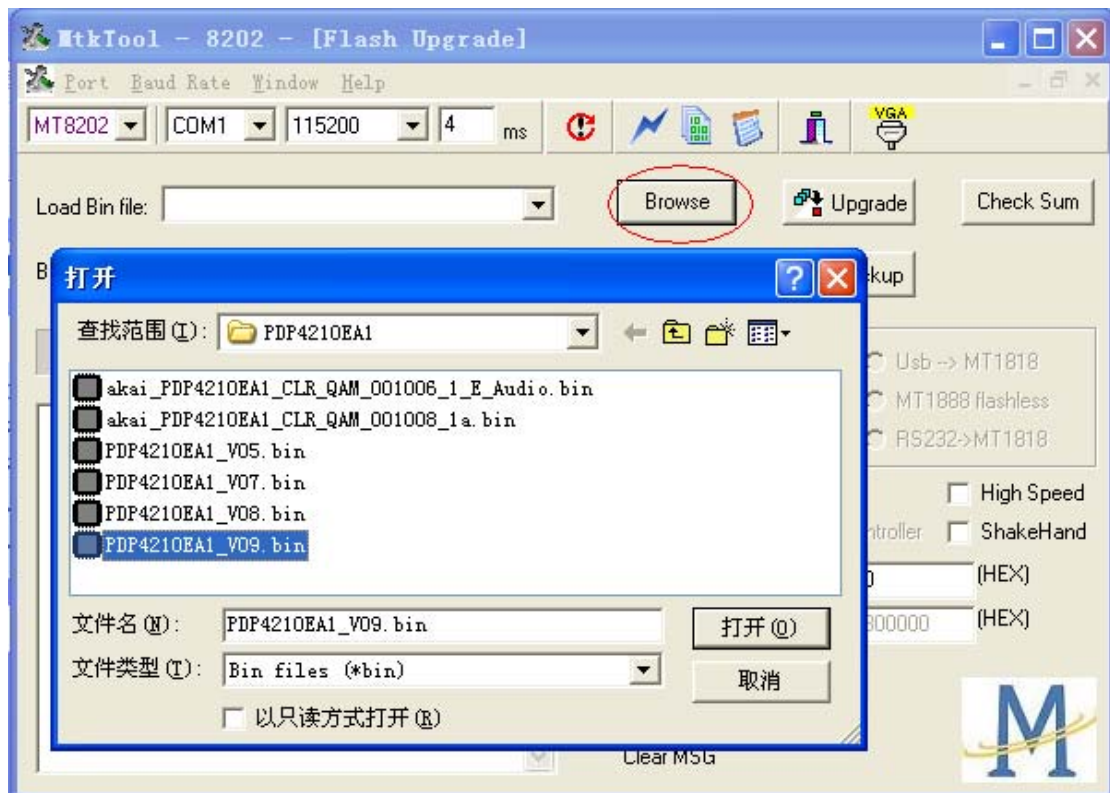
3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the TV will be standby mode if after turn on the main power only .)
4. Execute MTKtool and select the chipset as MT8202. (the software of MTKtool will be sent to your side)



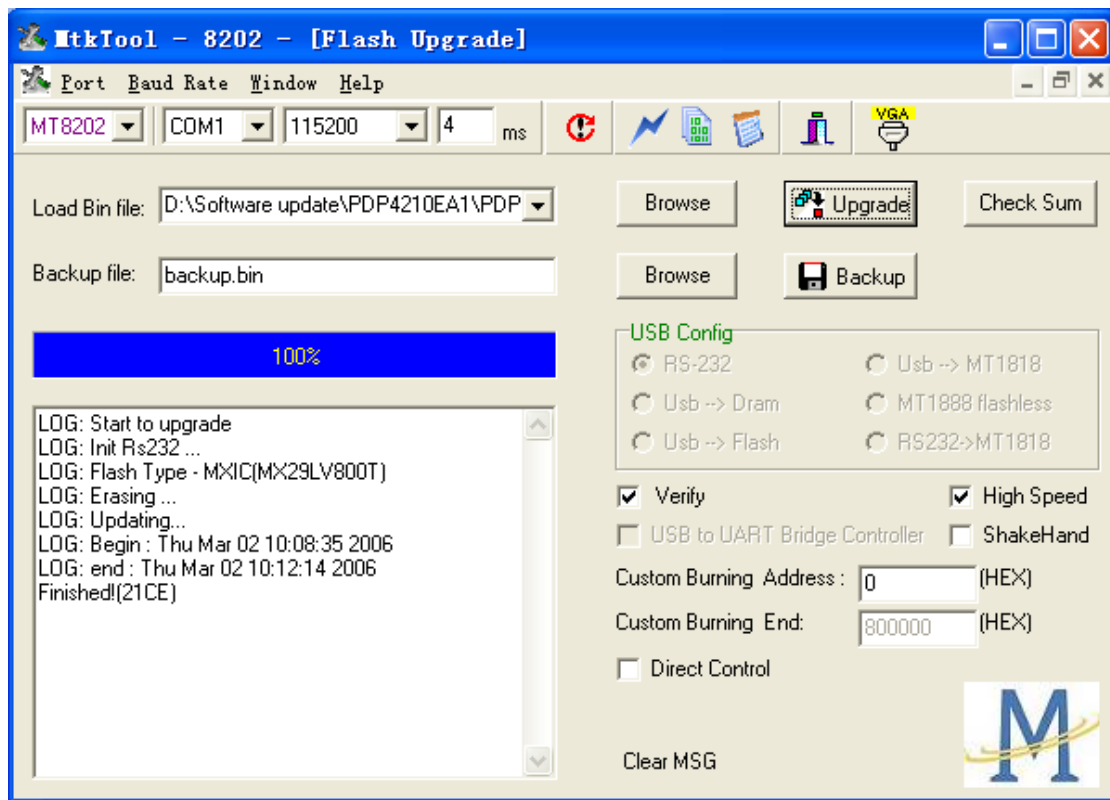
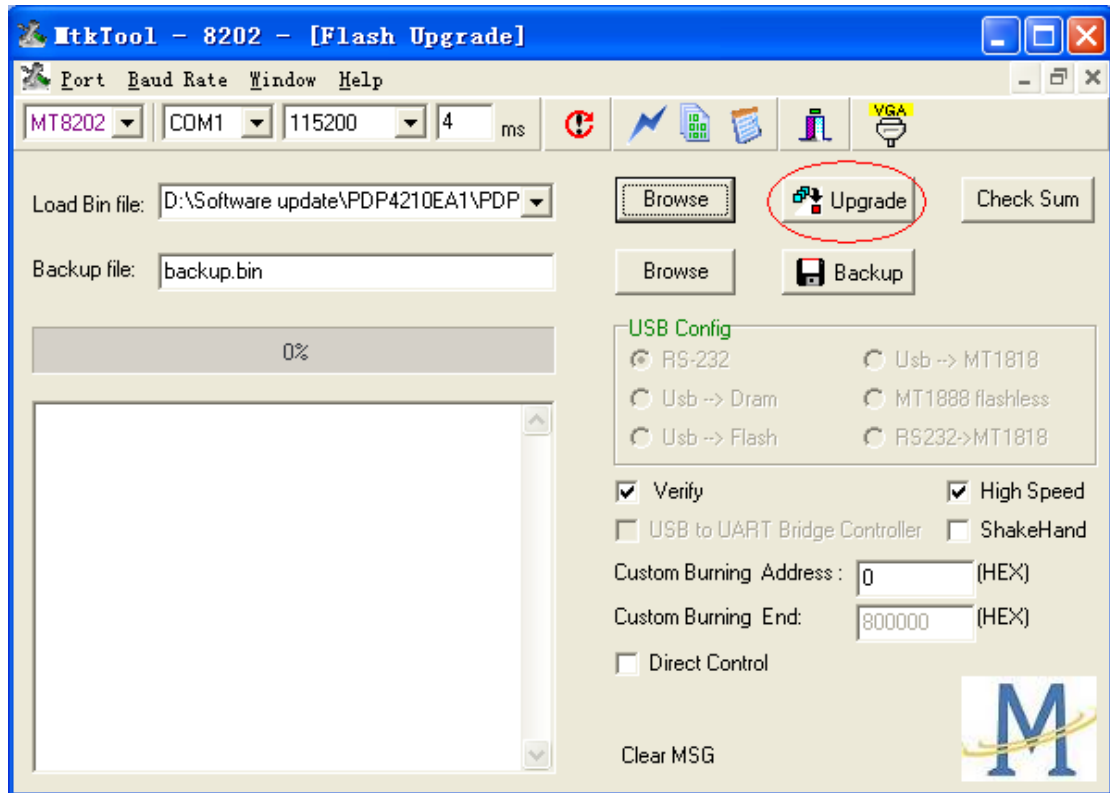
5. Select current COM port. (please try to check the COM port of your PC).



6. Choose the bit rate as 115200.
7. Select the update binary by pressing browse button. For example, the binary file name is PDP4210EA1_V09.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.



9. The update process is successful as the progress bar is 100%. After the update process is ok,

turn off power and wait indicator light is off. Turn on power and TV can work.

Checking

It is needed to check the version of the firmware for MT8202 which has been download into the Plasma TV .

Press Menu button of the remote control, following input “8202” of the remote control and OSD menu for Factory Setting is appeared on the screen .

Use the remote control and select the mode of Firmware Version and then enter the mode of Firmware Version . It is easy to be found the version of the current firmware for MT8202 is as the following : “Factory ID : PDP4210EA1_VXX ”

Appendix:

Quick Installation Guide For Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 – VGA cable (#4)
- USB cable x 1 (#5)

2. Installation for ATV upgrade

2.1 Connect RS232 cable (#2) to PC serial port



Connect another side of RS232 cable (#2) to the board (#1)



2.2 Connect RS232-VGA cable (#4) (RS232 side) to the board (#1)



Connect RS232-VGA cable (#4) (VGA side) to the TV



2.3 Connect USB cable (#5) to the board (#1)

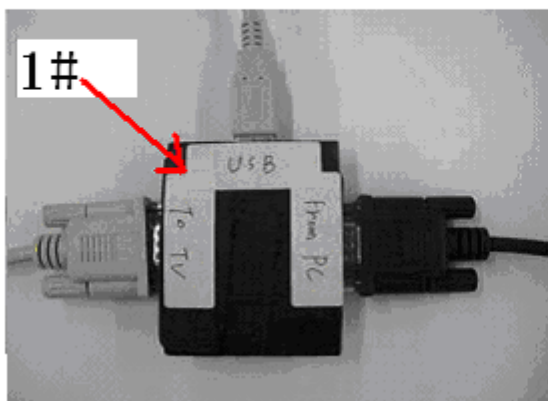


Connect another side of USB cable (#5) to PC

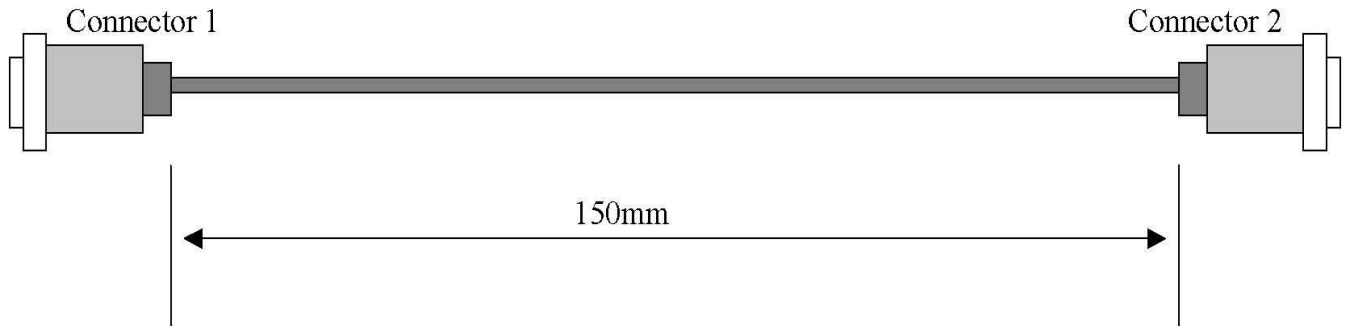


3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



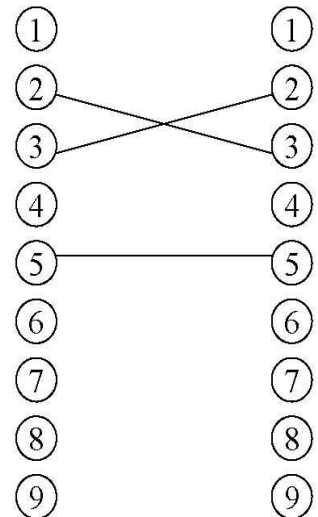
RS232 Null Cable for PC (#2)



Pin Assignment
Of DB9 Female

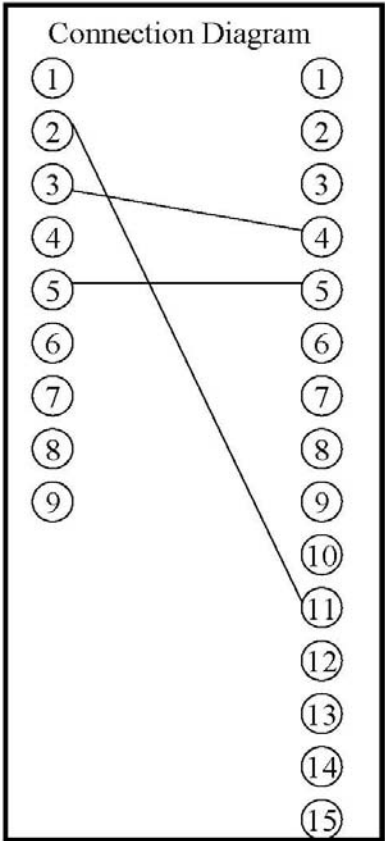
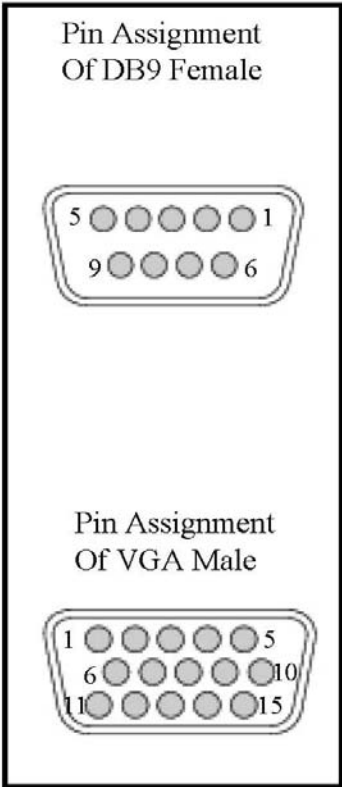
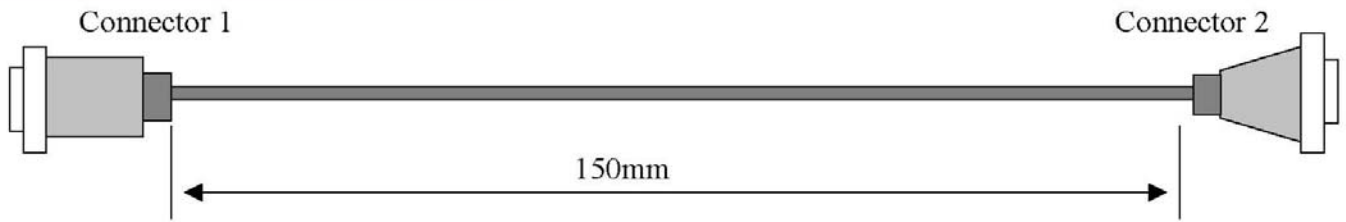


Connection Diagram



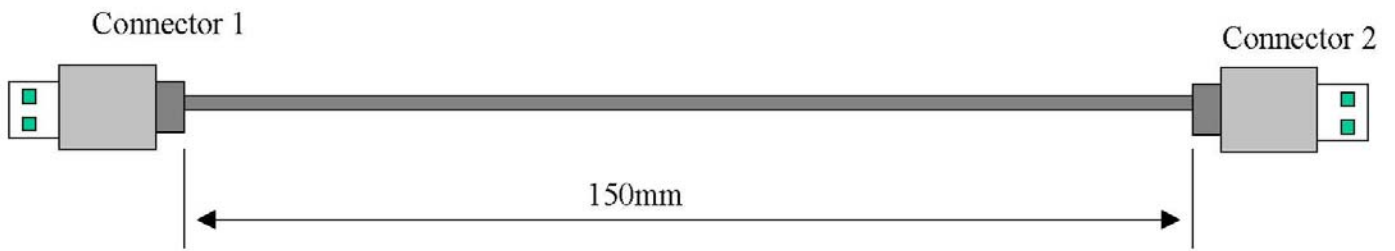
Connector 1: DB9 Female
Connector 2: DB9 Female

RS232 - VGA Cable (#4)



Connector 1: DB9 Female
 Connector 2: VGA Male

USB Cable (#5)



Connector 1: Standard USB Male

Connector 2: Standard USB Male

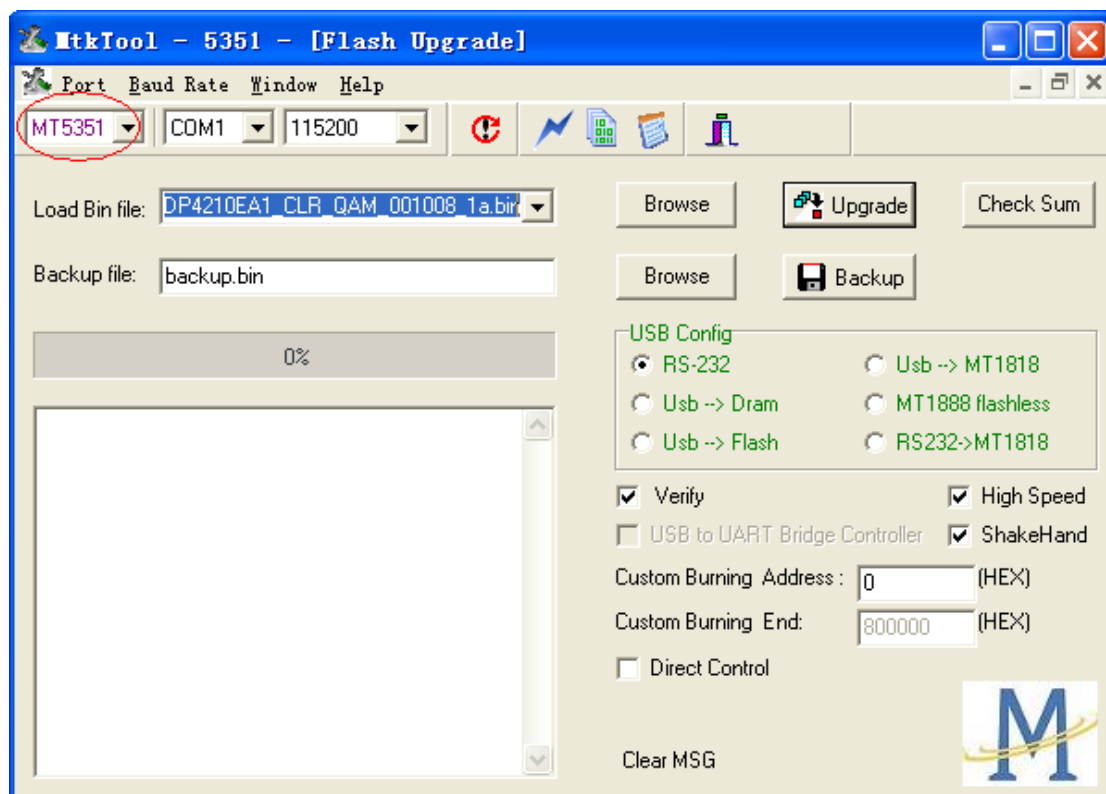
Process of update MT5351AG

Preparing :

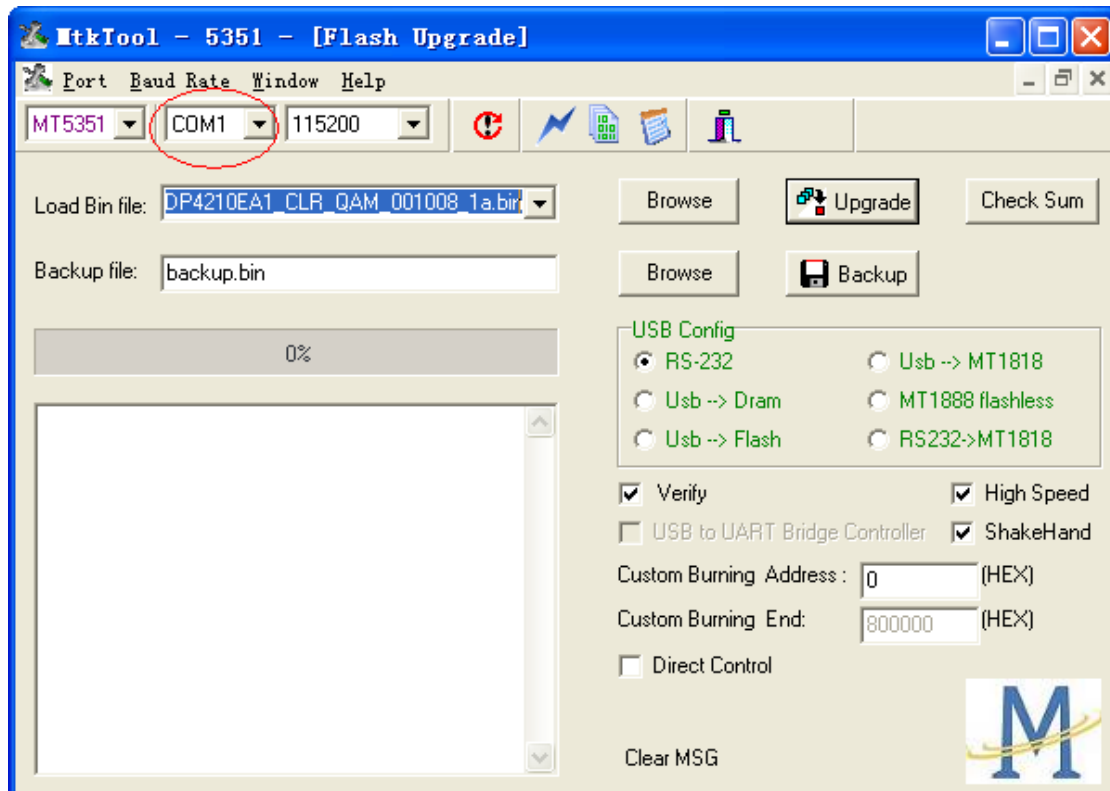
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**. Please find the details for connecting **referring to the appendix at the end of this file**.
2. Store the MtkTool into the PC

Downloading :

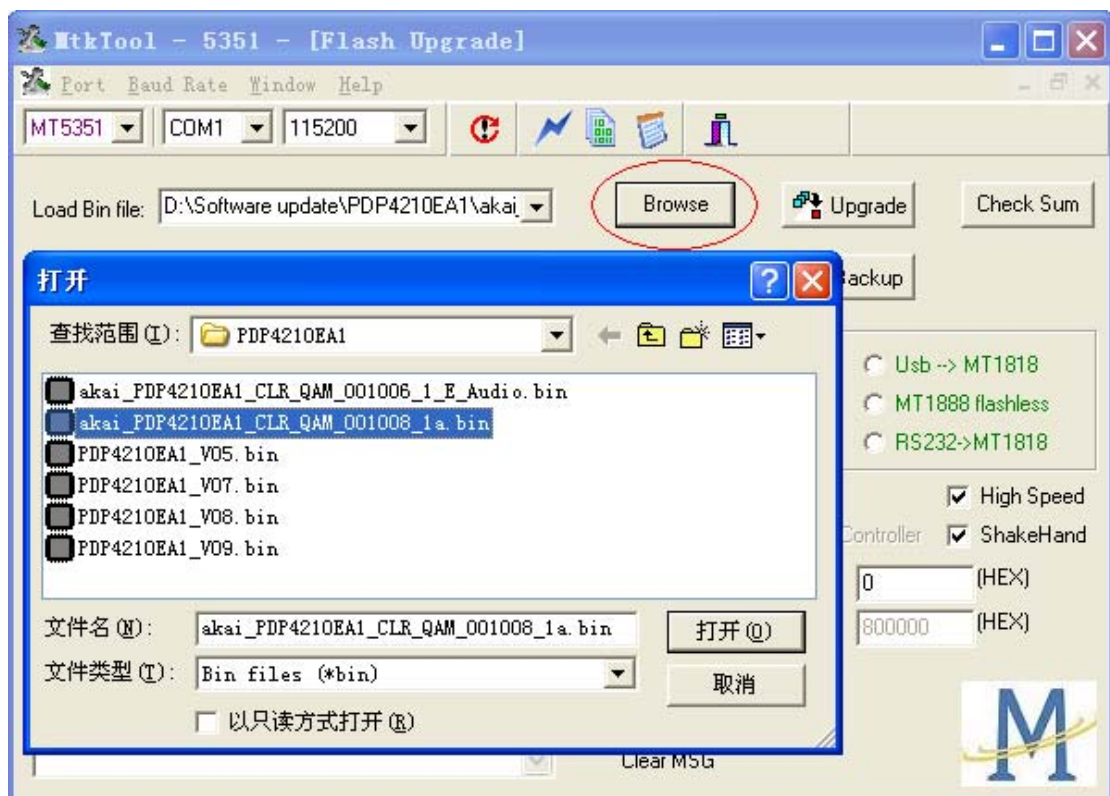
3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the TV will be standby mode if after turn on the main power only .)
4. Execute MTKtool and select the chipset as MT5351. (the software of MTKtool will be sent to your side)



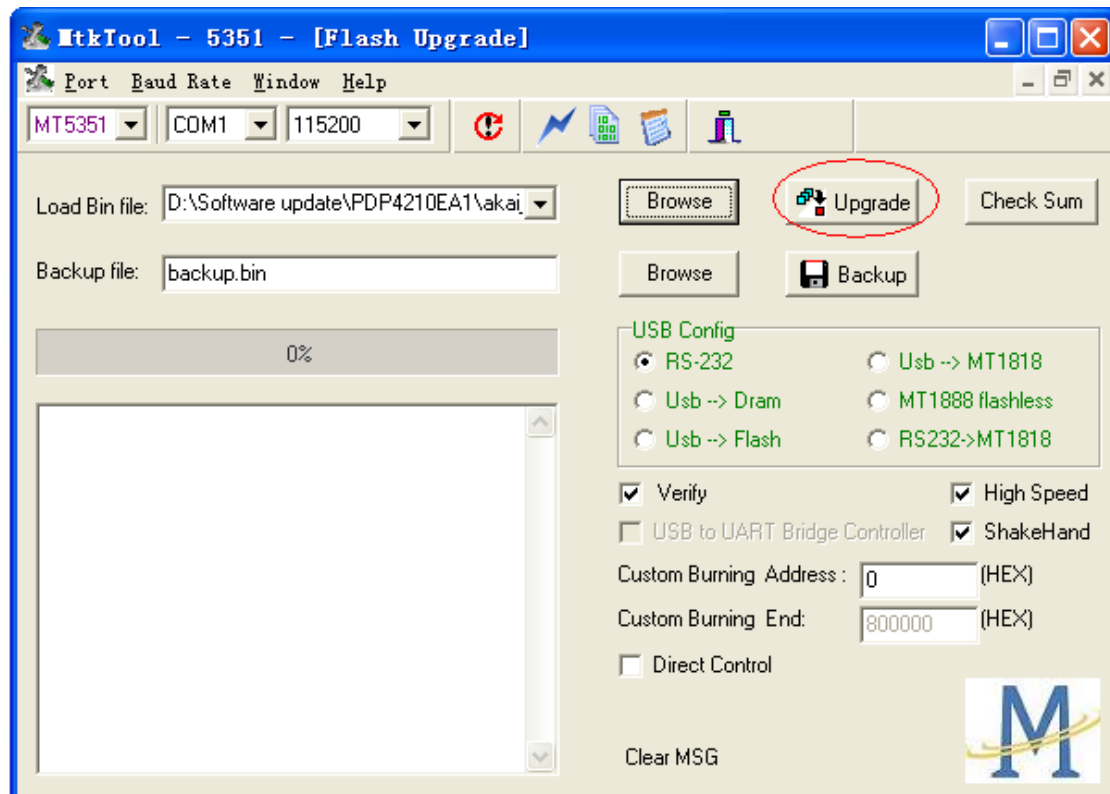
5. Select current COM port. (please try to check the COM port of your PC).



6. Choose the bit rate as 115200.
7. Select the update binary by pressing browse button. For example, the binary file name is XXXX_PDP4210EA1_000000XX_X_P.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.



9. The update process is successful as the progress bar is 100%. After the update process is ok, turn off power and wait indicator light is off. Turn on power and TV can work.

Checking :

It is needed to check the version of the firmware for MT5351AG which has been download into the Plasma TV .

Press Menu button of the remote control and the main OSD menu is appeared on the screen .

Use the remote control and select the DTV menu . following input “0000” (zero , zero , zero , zero) of the remote control .Then enter the mode of factory after input the digits .

It is easy to be found the version of the current firmware for MT5351AG is “PDP4210EA1 CLA_QAM_XXXXXX_XX”under the mode of factory .

Appendix:

Quick Installation Guide For Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 null cable x 1 for DTV (#3)
- USB cable x 1 (#5)

2. Installation for DTV upgrade

2.1 Connect RS232 cable (#2) to PC serial port



Connect another side of RS232 cable (#2) to the board (#1)



2.2 Connect RS232 cable for DTV (#3) to the board (#1)



Connect another side of RS232 cable for DTV (#3) to the TV



2.3 Connect USB cable (#5) to the board (#1)

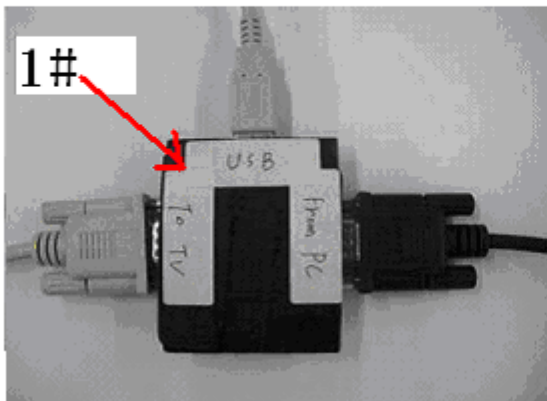


Connect another side of USB cable (#5) to PC

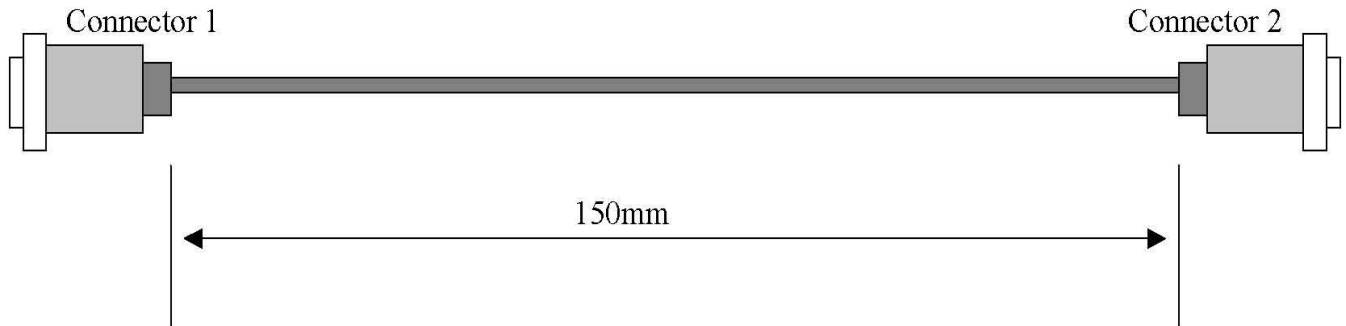


3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



RS232 Null Cable for PC (#2)

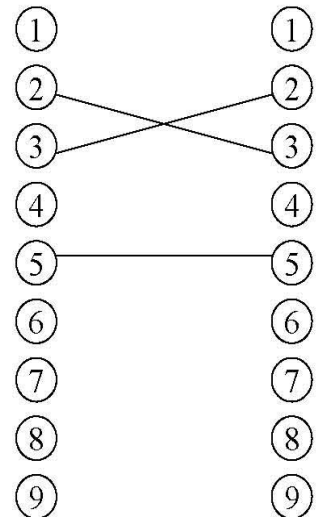


Pin Assignment
Of DB9 Female

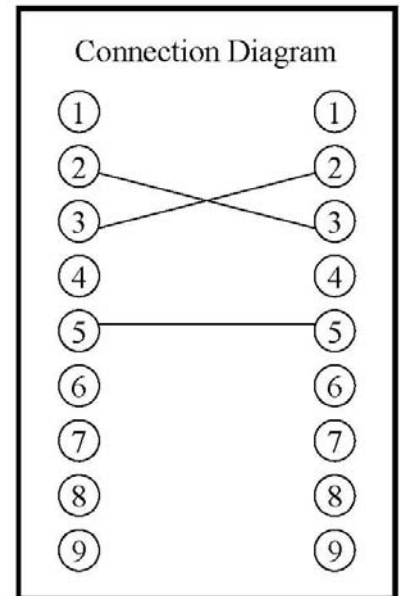
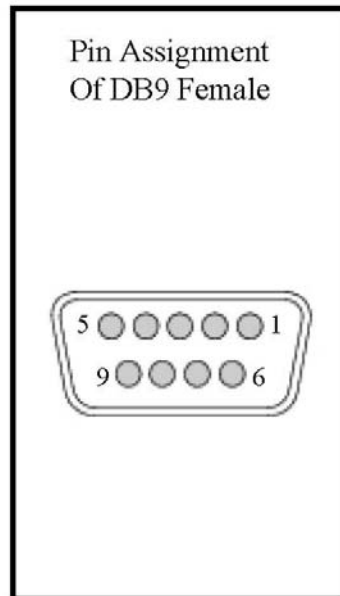
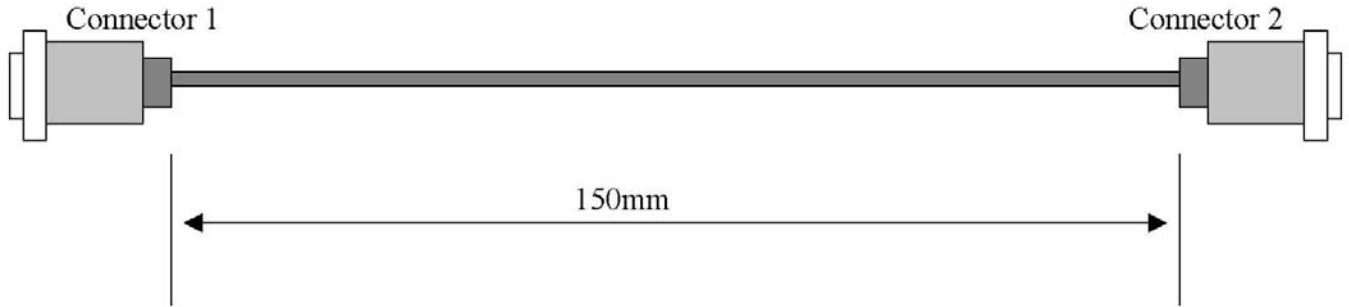


Connector 1: DB9 Female
Connector 2: DB9 Female

Connection Diagram

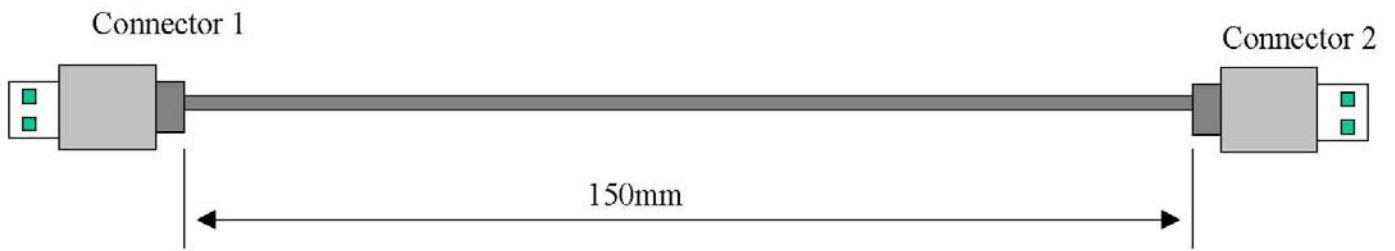


RS232 Null Cable for DTV (#3)



Connector 1: DB9 Female
Connector 2: DB9 Female

USB Cable (#5)



Connector 1: Standard USB Male

Connector 2: Standard USB Male